INVESTIGATION OF WIDE BAND GAP SEMICONDUCTORS: InGaZnO TFTs FOR CHEMICAL SENSING AND HYBRID GaN/ORGANIC HIGH-FREQUENCY PACKAGING AND CIRCUITS

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To my parents, Dimitris and Vasso Pavlidis, who have supported me from the beginning.

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Πάντες ἄνθρωποι τοῦ εἰδέναι ὀρέγονται φύσει...

ὅλως τε σημεῖον τοῦ εἰδότος καὶ μὴ εἰδότος τὸ δύνασθαι διδάσκειν ἐστίν...

All men naturally desire knowledge...

in general, what separates the man who knows from the man who does not know, is that the former can teach...

Aristotle, Metaphysics (350 BC)

SUMMARY

Wide bandgap semiconductors (WBG) are an attractive class of materials that offer a number of performance advantages over traditional silicon (Si). Examples of their superior properties include high electron mobility, temperature stability, high breakdown voltage for increased power handling, and transparency in the visible wavelength spectrum. It is envisaged that these properties can be exploited to realize the high performance electronic systems of the future.

In this work, two application areas have been investigated: 1) chemical sensing and 2) radio-frequency (RF) communications. The chemical sensing thrust has been addressed with the fabrication of indium gallium zinc oxide (InGaZnO) thin film transistors (TFTs) using low temperature processes. Whereas previous works have relied on high temperature fabrication and/or device operation that are incompatible with flexible and low-cost substrates, this work successfully exploits low temperature microfabrication methods to manufacture InGaZnO TFTs for chemical sensing at room temperature. Gas-phase sensing of volatile organic compounds is demonstrated, and it is shown that sensitivity can be improved through the use of a polymer capping layer. For liquid-phase sensing, reliable passivation remains a challenge. In response, this work shows that low temperature atomic layer deposition of TiOx can be used to create dual-gate InGaZnO TFTs with Super Nernstian pH sensitivity and long term reliability within a liquid environment. An alternative approach to liquid sensing is also studied, wherein a InGaZnO phototransistor is deployed to capture the light emitted from a Zn-ion sensitive photoluminescent polymer, thus alleviating the need to place the TFT in contact with a liquid.

Another wide bandgap semiconductor, gallium nitride (GaN), has been explored for wireless applications, particularly in the X-Band (8-12 GHz), where it has enormous potential for use in weather and military radar systems. However, the majority of GaN RF amplifier circuits so far have either been limited to monolithic demonstrations, or relied

on expensive packaging materials. Low-cost, low-loss, and multi-layer organic laminate materials, in particular liquid crystal polymer (LCP), are investigated for GaN packaging for the first time. Due to the high power operating levels associated with GaN devices, and the low thermal conductivity of these organics, it is found that traditional packaging techniques place significant limits on GaN's electrical performance. To counter act this, a novel encapsulated flip-chip package in LCP has been conceptualized. It is found that not only does the package provide adequate thermal management for multi-watt performance, but the use of of flip-chip bonding also minimizes interconnect parasitics and facilitates wideband amplifier design. As proof of this package's viability, a hybrid X-Band power amplifier (PA) has been designed and measured, showing 5.4 W of output power (P_{OUT}) under continuous wave (CW) operation, or 7 W under pulsed conditions with δ = 50%. Despite the high-power advantages of GaN, entire RF systems cannot be with it alone. Therefore, the encapsulated package technique has been extended to permit the integration of heterogeneous semiconductor components. A hybrid receiver front-end is realized on multi-layer Rogers 3003™ to demonstrate this concept, incorporating a flip-chip bonded SiGe low noise amplifier (LNA) and a ribbon-bonded GaAs mixer. This is the first time that heterogeneous semiconductor technologies have been integrated within a multi-layer organic package using different interconnects for each chip to form a receiver. Moreover, the receiver achieves the widest bandwidth among heterogeneous receivers reported to date.

Thus, the objective of this research is to investigate the use of wide bandgap semiconductors, in particular InGaZnO and GaN, for chemical sensing and wireless electronics, respectively. Several key factors are considered: device fabrication, thin film and device characterization, thermal and RF packaging, circuit design and system integration.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Silicon (Si) has long reigned in the world of electronics. Driven by Moore's Law [1], the number of Si transistors per area has doubled every two years since 1970, reaching previously unimaginable levels of integration. The current state-of-the-art 14 nm technology node, which was commercially made available in late 2014/early 2015 [2, 3], has a channel length less than 100 individual Si atoms across. As a result, Intel's newest Broadwell processor boasts 1.9 billion transistors within a 133 mm^2 die area [4]. Despite the incredible technological and commercial achievements of Si-based electronics, there remain applications where Si falls short and alternative materials must be considered. Two of these applications, namely flexible/transparent chemical sensors and high-power, high-frequency electronics, are explored in this thesis.

1.1.1 Flexible, Wearable and Transparent Chemical Sensors

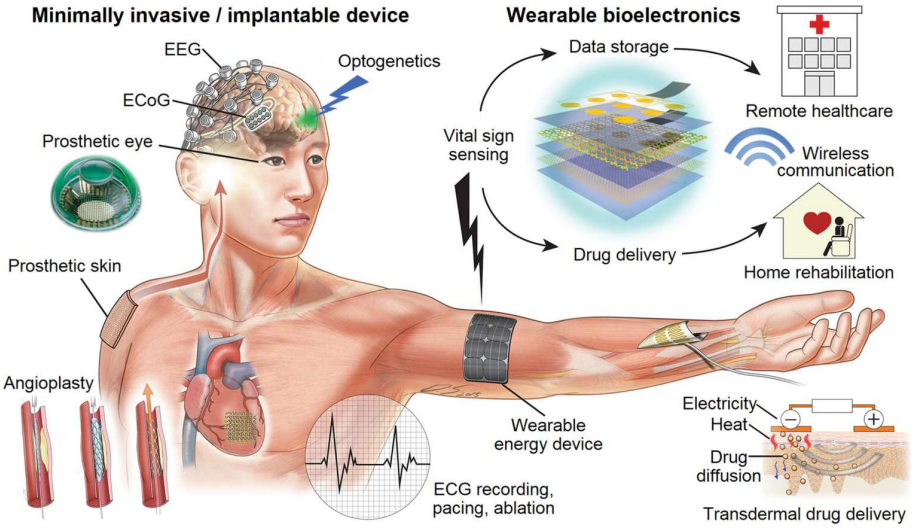
Conventional biomedical and environmental chemical analysis often consists of collecting samples at the point of interest and then sending them to an off-site facility for analysis. The advantage of this approach is that state-of-the-art analytical equipment can be used at the off-site facility to provide highly sensitive results. The drawbacks, however, are numerous: (1) increased time required to obtain results, (2) increased cost due to the necessity for sample collection and transportation, and (3) increased risk of sample spoilage that could compromise the validity of the analysis altogether. To avoid these issues, there is a need for chemical sensors that can yield results at the point of care (POC) itself.

The need for portable sensors in general, both chemical and otherwise, has driven the commercialization of wearable sensors that track basic activity indicators, such as temperature, heart rate and physical motion (e.g., step counters) on the go [5]. To do this, today's

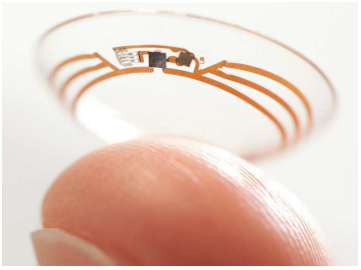
systems employ rigid silicon chips that are integrated on flexible circuit boards. To obtain a more detailed understanding of an individual's condition, however, chemical markers will also need to be tracked in the future. In athletes, monitoring electrolyte concentrations can indicate and avoid the onset of dehydration [6]. Additionally, blood sugar sensing can help manage diabetes, a disease that affects more than 422 million people globally and is responsible for 1.5 million annual deaths [7].

The rigidness of Si, however, makes it difficult to create chemical sensors that sit directly on and conform to the complex and dynamically changing curvature of human skin, as would be required to continuously collect bio-samples without user intervention. Therefore, it is desirable to develop sensors and electronic platforms made from bendable and/or stretchable materials (see Figure 1.1a). The recently demonstrated "smart contact lens" in Figure 1.1b by Google X serves as an illustrative example of the aforementioned challenges [8]. Though the lens itself is flexible, rigid Si chips were used for the on-board circuitry that increase the risk of eye abrasions and obstruct vision. The latter introduces a further trait that should be considered: optical transparency.

As both sensors and other types of electronics become more ubiquitous in our daily lives, there is a trend to integrate them so heavily into our surrounding environments that they essentially become invisible. This can be accomplished through miniaturization, as has been done in the past several decades, as well as through the use of inherently transparent materials. Consequently, simple objects, such as windows, can be transformed into active devices (e.g., environmental air quality monitors) within the home or workplace without compromising their original functionality (see Figure 1.1c) [10]. Transparent conductors, such as indium tin oxide (ITO), and transparent dielectrics, such as plastics, that can be used for these applications are readily available. The study of high performance and transparent semiconductors that can be deposited at low temperatures on flexible and low-cost substrates still merits investigation for chemical sensing.



(a)



(b)

(c)

Figure 1.1. (a) Flexible and wearable electronics (e.g., sensors, energy harvesters, actuators, etc.) for human performance monitoring. [9], (b) contact lens with with integrated glucose sensor [8], (c) smart windows of the future [10].

1.1.2 High-Power and Wideband μm- and mm-Wave Electronics

High frequency electronics play a key role in our lives, blending into the infrastructure around us to enable a range of applications, from consumer telecommunications to atmospheric spectroscopy to military and weather radar. As depicted in Figure 1.2, the radio spectrum has become very crowded. Well-established technologies, such as AM/FM radio, WiFi and 3G cellular networks operate below 3 GHz. New applications that require high data rates (i.e., 5G cellular networks) are moving to higher frequencies where there is more bandwidth. Moreover, meteorological radar, military radar, as well as many space/satellite-related communications (e.g., NASA's Deep Space Network) operate in the X-Band (8-12 GHz).

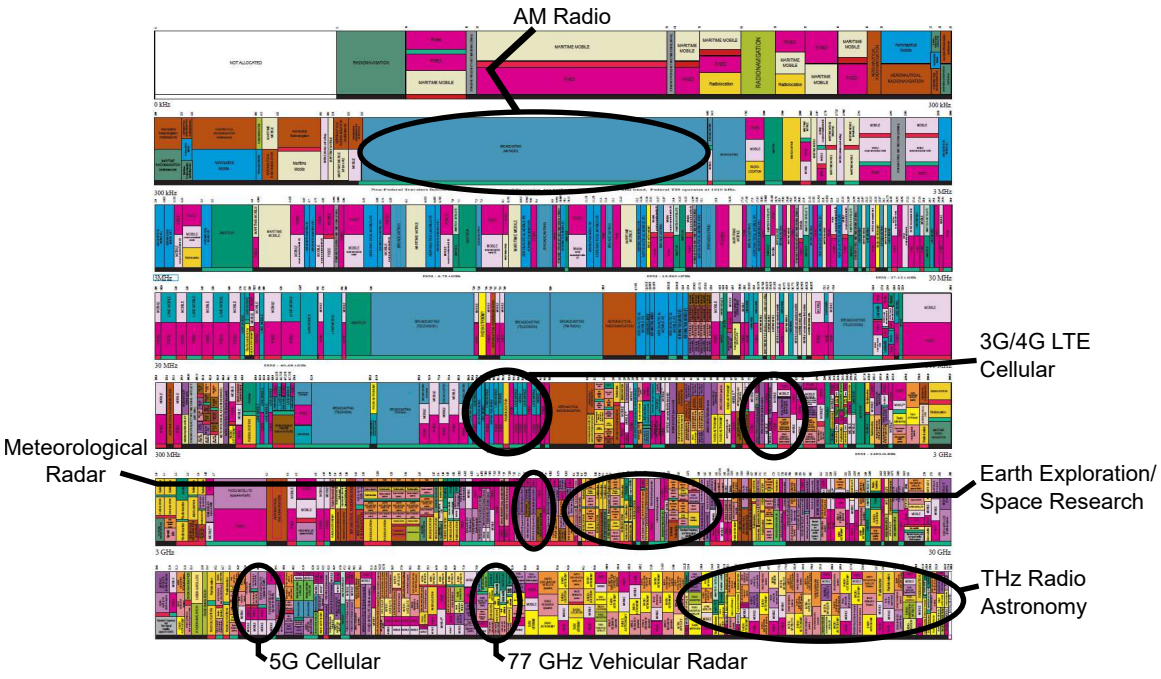


Figure 1.2. Radio frequency spectrum allocations as defined by the U.S. Department of Commerce, ranging from 3 kHz up to 300 GHz. The spectral allocations for some popular commercial and research applications are labeled. Adapted from [11].

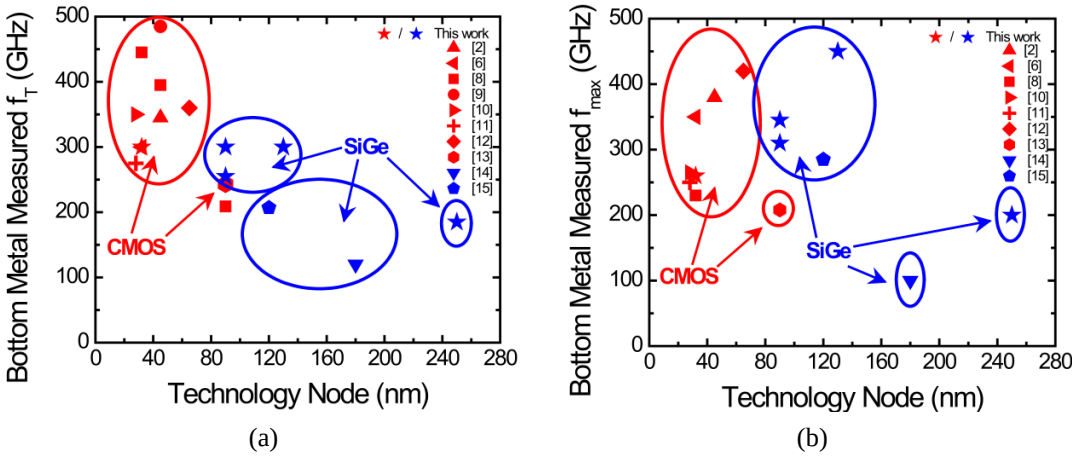


Figure 1.3. Comparison of (a) f_T and (b) f_{max} between Si nFETS and SiGe HBTs. [12]

The frequency performance of a device can be benchmarked by two parameters: the unity-gain frequency (f_T) and the maximum oscillation frequency (f_{max}). In Figure 1.3, silicon n-channel field effect transistors (nFETs) are compared with their close cousin, silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) [12]. nFETs have benefited from aggressive miniaturization, with recent nodes recording f_T in the 400-500 GHz range.

However, it can be seen that for the same technology, SiGe HBTs achieve a higher f_T than Si nFETs. In terms of f_{max}, SiGe HBTs match Si nFETs at larger nodes, which facilitates fabrication. It is therefore expected that as the technology node of SiGe advances, it will surpass the limits of Si. This trend raises the question of whether entirely different material classes can be leveraged to reach even higher frequency ranges.

In addition to the frequency of operation, a critical parameter in the success of any RF system is power, as it determines the distance over which a signal can be sent and received successfully. Traditionally, high power amplifiers have been made using vacuum-based traveling wave tubes (TWTs) [13]. This technology has matured to become highly reliable, but suffers from low levels of integration due to the bulky components that are used. To overcome this hurdle, solid-state power amplifiers (SSPAs) will need to be developed. Overall, next generation high frequency electronics will need to operate at both high frequencies and high powers.

1.2 Survey of Wide Bandgap Semiconductors

The above discussions make it clear that there exist a number of emerging applications that require unique performance traits not available to Si, such as low-temperature processing for compatibility with flexible substrates, transparency in the visible regime and high-power micro- to mm-wave operation. Where Si falls short, however, other semiconductors can take its place. One such class of materials is wide band gap (WBG) semiconductors. WBGs can be broadly defined as semiconductors whose band gaps (E_G) are "significantly greater than those of silicon" [14], usually greater than 3 eV. This distinction is best clarified through a comparison of electronic material properties. Out of the five materials shown in Table 1.1, Si and GaAs (gallium arsenide) are considered conventional semiconductors, whereas SiC (silicon carbide), GaN (gallium nitride) and ZnO (zinc oxide) are all wide band gap semiconductors. The breakdown electric field strength (E_B), which is a measure of the upper limit of voltage that a device made from the semiconductor can operate under, is

Table 1.1. Comparison semiconductor crystalline material properties (at T = 300K). Data taken from references [15–19].

Property	Si	GaAs	SiC	GaN	ZnO
Band Gap, E_G [eV]	1.12	1.42	3.25	3.4	3.2
Breakdown Field, E_B [MV cm^{-1}]	0.25	0.4	3	4	2-4
Electron Mobility, μ [cm^2 V^{-1} s^{-1}]	1350	6000	800	1300-2000	200
Maximum velocity, ν_s [10^7cm s^{-1}]	1	2	2	3	3.2
Dielectric constant, ϵ	11.8	12.8	9.7	9	7.8

proportional to the band gap. Critically, the electron mobility (μ) and maximum/saturation velocity (ν_s) of WBG semiconductors are not greatly reduced compared to Si and GaAs, particularly in the case of GaN. The dielectric constant (ϵ) plays an important role in circuit design by affecting the metal line impedances in high frequency transmission lines.

Due to their advantageous properties, SiC and GaN have begun to dominate power electronics, where high voltage operation can be sustained in tandem with kHz to MHz switching frequencies for increased system efficiency [20–22]. GaN, in particular, has also been targeted for high power micro-wave to millimeter-wave communications systems [23, 24]. Unlike Si, GaN is a piezoelectric material – its piezoelectric coefficient (c_{33}) is +0.65 C m^{-2} – which makes it an interesting material for microelectromechanical systems (MEMS) [25]. Where GaN has achieved greatest commercial success, however, is in solid-state lighting [26–28]. Its direct wide band gap has given rise to high-brightness and high-efficiency blue light emitting diodes (LEDs), which have enabled the development of solid-state lighting. Overall, the growth of GaN-based electronics and optoelectronics has had a dramatic effect on semiconductor and defense companies, such as Qorvo, Macom Raytheon, Northrup Grunman and Cree. Some predictions cite double-digit growth in the coming years, with a market revenue for RF applications reaching $560 million by 2019 [29]. Cree, in particular, has found great success by competing simultaneously in the lighting, RF and power device markets through its combined expertise in both GaN and SiC. In 2014 alone, it recorded $1.6 billion in overall revenue, 47% coming from LED sales alone [30].

ZnO is a II-VI compound with attractive properties for a variety of applications. Its

band gap is similar to GaN's, and while its μ is lower, it has a slightly higher v_s, which means that it can still be used for some high frequency applications. ZnO's breakdown field is still a point of debate in the literature, however due to its E_G being so close to GaN's, it is predicted that its E_B must also be similar [19]. As a metal oxide, ZnO has long been of interest for gas sensing applications as well, both in thin film and nanowire form [31–33]. It has also been investigated for lighting and lasers, due to its direct band gap structure, but challenges in reliably growing p-type films has limited its potential in this area [34–36]. A new and growing role for metal oxides is as the semiconducting active layer in thin film transistors (TFTs), particularly for transparent electronics/display applications [37, 38]. The driving force behind this trend is two-fold: 1) high optical transparency in the visible wavelength range, and 2) higher electron mobilities than amorphous Si deposited at low temperatures. Regarding the latter, ZnO TFTs with f_T / f_{max} of 2.45 GHz/7.45 GHz were fabricated using pulsed laser deposition (PLD) with a maximum process temperature of only 400°C [39].

In summary, WBG semiconductors offer a range of advantageous properties compared to Si. Due to their optical transparency in the visible regime and high mobility even when deposited at low temperature, metal oxide TFTs are considered as candidates for flexible electronics. Moreover, GaN high electron mobility transistors (HEMTs) are considered for high-power and high-frequency applications due to their large mobility and large breakdown field strength.

1.3 InGaZnO Thin Film Transistors for Chemical Sensing Applications

In this section, thin film transistors (TFTs) will be briefly introduced, and different semiconductor materials for TFTs will be compared. A more-in depth description of TFTs and their operation is provided in Chapter 2. TFTs are switch-like electronic devices made up of individually deposited and patterned heterolithic thin films. This is in contrast to

conventional monolithic semiconductor processing, wherein a single element is manipulated to produce each functional layer in the device (i.e., n- or p-type Si semiconductor, SiO_2 dielectric, poly-Si contacts, etc.). The freedom of incorporating different materials makes it possible to use different deposition techniques (some inherently well suited for low-cost mass production), to adjust process temperatures so that flexible and low-cost substrates such as glass and plastics can be used, as well as to tune optical transparency to create flexible, transparent devices. The main application of TFTs lies in flat panel displays [40, 41] where the TFT modulates one or more LED(s). Additional applications have also been explored, including light [42–44] and x-ray detection [45–47], in addition to chemical sensing, which will be discussed below.

Table 1.2 contrasts the typical performance of the most popular semiconductor material technologies used to fabricate TFTs. Hydrogenated amorphous (a-Si:H) and polycrystalline (poly-Si) silicon represent the two most widely used traditional technologies for these devices. Due to the maturity of silicon technology, it is possible to dope the films for either n-type or p-type behavior. While poly-Si offers best-in-class electron mobility, it is deposited at high temperatures that make it incompatible with affordable glass substrates. a-Si:H, on the other hand, decreases the process temperature at the significant cost of carrier mobility. A further limitation of these materials is that they are not greatly transparent at visible wavelengths, which is of importance when manufacturing a display unit.

Organic TFTs (OTFTs), which are generally p-type, have gained much attention due to their low-cost, stemming from the materials that are inherently used, as well as the mass-production-friendly processes that can be leveraged to create these devices (i.e. ink-jet printing and spin-coating) [52–55]. This has permitted their implementation on a variety of low-cost and flexible substrates, such as glass, plastics and paper. When deposited at room temperature, they are typically amorphous with comparatively low hole mobilities ≤ 1 cm^2 V^{-1} s^{-1}. However, it has been shown that high temperature deposition of organics can turn them polycrystalline and thereby offer higher mobility (i.e., 25 cm^2 V^{-1} s^{-1}) [53].

Table 1.2. Comparison of typical TFT semiconductor material performance based on different semiconductors. Data taken from [39, 48–51]

Property	a-Si:H	poly-Si	Organics	ZnO	InGaZnO
Majority Carrier Type	n/p	n/p	p	n	n
Carrier Mobility, μ [$cm^2\ V^{-1}\ s^{-1}$]	0.5-1	30-300	≤1	20-70	3-35
Process Temperature [°C]	350	450	≥R.T.	≥R.T.	≥R.T.
Visible-Light Transparency [%]	<20	<20	>80	>80	>80
Crystal phase	A*	P*	A*	P*	A*
Compatible Substrates	Glass	Quartz	Glass Plastic Paper	Glass Plastic	Glass Plastic Paper

*A: amorphous, P: poly-crystalline.

The non-room temperature deposition of a-Si:H, along with the relatively low mobility of both a-Si:H and organic TFTs, motivate the investigation of metal oxide-based TFTs. These materials are largely n-type (exceptions such as copper oxide, CuO, exist however [56]) and have been integrated with OTFTs to form inverters [57, 58], the basic building block of digital logic electronics. ZnO, which can be deposited via PLD, R.F. sputtering [59] or atomic layer deposition (ALD) [60, 61], is the most traditional of these materials with high mobility and high visible wavelengths transmittance. Though it can be deposited as low as room temperature, its polycrystalline film structure introduces grain boundaries that can compromise uniformity and stability over large areas [62]. Its close cousin, indium gallium zinc oxide (InGaZnO or IGZO) – a wide band gap semiconductor with E_G = 3.2 eV – is amorphous when deposited at room temperature and still offers larger mobilities than a-Si:H and organics [63]. Moreover, it has been reported that ZnO TFTs degrade greatly when subjected to bending, while InGaZnO TFTs experience minimal change in performance under similar conditions [64]. These properties make InGaZnO a highly attractive technology for high-performance and flexible electronics. In fact, InGaZnO TFTs have been rapidly developed by both industry and academia in recent years to achieve high-resolution, as well as flexible and roll-to-roll printed displays [65–70].

Given the rise of transparent, high performance and flexible InGaZnO TFT circuits, the

successful development of InGaZnO TFT-based chemical sensors would altogether address the shortcomings of traditional Si electronics as presented in Section 1.3, and give way to a new wave of flexible biochemical sensors. Chemically sensitive resistors (chemiresistors) have been made with InGaZnO for gas-phase sensing with limits of detection in the 100 ppb to low ppm ($\sim 12 - 15 ppm$) ranges [71, 72]. However, these devices were either operated at high temperatures (~350°C) or required high temperature InGaZnO thin film deposition (≥200°C), which conflict with the main advantage of InGaZnO: low-temperature manufacturability and operation on low-temperature, low-cost substrates. More interestingly, a room-temperature InGaZnO TFT-based gas sensor with a limit of detection in the range of 1-10 ppm has been reported [73]. In this case, the TFT was capped with semiconducting organic polymers poly(3-hexylthiophene) (P3HT) and copper phthalocyanine (CuPc) to enhance sensitivity to ammonia and nitric oxide gases. However, in light of the fact that these polymers exhibit their own sensitivity to such gases [74–76], it is difficult to assess the contribution of the InGaZnO to the sensitivity.

In terms of liquid-phase sensors, pH sensing is important in itself, but also serves as a good benchmarking tool for more complex biochemical analytes. Traditionally, the maximum sensitivity of FET-based pH sensors is defined by the Nernst Limit, which is 59 mV/pH. That is, that for every unit change of pH, the threshold voltage of a device changes by up to 59 mV [77, 78]. Dual-gate TFTs have been developed using organics, ZnO and InGaZnO [79–82] whose sensitivities exceed this limit. Though sensitivities as high as 2.25 V/pH have been shown, all of these works share a common shortcoming: they rely on thick, thermally grown SiO_2 bottom gate dielectrics. As with the gas sensors above, the high temperatures required to obtain this oxide layer undermine the low-temperature advantages of InGaZnO.

Lastly, thin film passivation of InGaZnO TFTs remains a critically important issue, as it can improve both bias stress [83] and environmental [84] stability, as well as permit the

deployment of these devices within a liquid medium for bio-chemical sensing. Nonetheless, it has been shown that passivation layers can also have deleterious effects on the TFT's performance [85]. Therefore, it is important to further study the source of these effects and develop suitable low-temperature passivation methods.

1.4 Gallium Nitride HEMTs for High Power Radio-Frequency Amplifiers

Though SiC and GaN have similar electron mobilities and maximum saturation velocities in bulk, GaN's true advantage is that it can form an AlGaN/GaN heterojunction in order to produce a two-dimensional electron gas (2DEG). From a device perspective, this means that SiC can only be used in metal-semiconductor field effect transistors (MESFETs), whereas GaN can be used to create high electron mobility transistors (HEMTs) [23]. HEMTs combine the advantages of high carrier concentration and high carrier mobility to increase output current and operation frequency for high power RF applications.

In the last decade, the performance of GaN HEMTs has increased rapidly. In 2005, >10 W mm^{-1} power densities were demonstrated at 40 GHz [86]. This was soon followed by the achievement of peak output powers of >1 kW at 3.2 GHz [87]. Frequency has also scaled quickly, with >300 GHz $f_T/fmax$ reported in 2010 by MIT/Raytheon researchers [88]. Triquint then demonstrated similar performance, but achieved this consistently across a 1000 transistor-level circuit [89], while HRL recorded >400 GHz $f_T/fmax$ using a 20 nm self-aligned gate (SAG) technology in 2013 [90]. Though the above examples focus on the development of GaN-on-SiC technology, it should be noted that the more affordable GaN-on-Si approach has also rapidly advanced [91–93].

In applications such as radar, electronic warfare, software-defined radio, and high data-rate communications, bandwidth is a critical parameter. Table 1.3 summarizes wideband GaN-based PAs that have been developed using both monolithic microwave integrated circuit (MMIC) and hybrid approaches, and have operational frequencies either within or

overlapping with the X-Band (8-12 GHz). It is seen that optimum performance, both in terms of bandwidth and large signal performance, is achieved using MMICs. Nonetheless, due to the increased cost of MMICs, the potential for passives with lower loss on low-ϵ boards, and heterogeneous integration, there remain strong incentives to investigate hybrids.

Until now, hybrid PAs have mainly been realized using wire-bond (WB) interconnects. This has two advantages: 1) simple and rapid prototyping, and 2) the backside of the GaN device can be mounted onto a good thermal conductor (e.g., copper) to serve as a heatsink. The majority of examples use ceramic substrates, such aluminum nitride (AlN) or alumina, which are brittle and relatively expensive compared to traditional printed circuit board (PCB) materials. In cases where multilayer substrates have been used, such as Rogers RO4003^{TM}, the GaN devices were wire-bonded, while the backside was mounted onto a separate heatsink. The disadvantage of wire-bonds is that they increase the electrical length of the interconnect, in turn increasing parasitics and limiting the achievable bandwidth of a hybrid PA. The flip-chip approach overcomes this problem using shorter metallic interconnect bumps, but raises the issue of heatsinking since the backside of the die is left unconnected. For this reason, flip-chip GaN PAs have only been demonstrated on AlN due to its high thermal conductivity [94, 95]. Thus, a strategy for flip-chip packaging high power GaN devices and PAs in low-cost multi-layer laminates is desired.

1.5 System-on-Package using Multilayer Organics

It is envisioned that next-generation systems will feature heterogeneous semiconductor integration, meaning that different semiconductor technologies will be assigned to each functional block, depending on their respective strengths (i.e., low-noise performance, mixed-signal integration, high power operation, etc.). Thus, monolithic systems on chip (SOC) cannot satisfy this objective. The three-dimensional system-on-package (3D-SOP) approach allows for both mixed semiconductor actives and passives to be embedded in the

Table 1.3. Comparison of wideband GaN PA performance.

	Technology	Topology	Freq [GHz]	P_{OUT} [dBm]	P.A.E. [%]
[96]	MMIC	DPA	2-18	38-42.5[1]	12-39
[97]	MMIC	DPA	2-20	39.9-43.3[1]	15.3-35.7
[98]	MMIC	Multi-stage	6-18	20-40.3[1]	10-24
[99]	MMIC	Reactive	8-18	32-33	24-34
[100]	WB-AlN	Power Combined	9.5	38.1 [3]	44
[101]	WB-ML	Power Combined	8-12	42-44[3]	55-60
[102]	WB-ML	Reactive	0.3-8	38-39[3]	23-36
[103]	WB-C	Power Combined	9.25-11.25	40-43 [3]	30
[94]	FC-AlN	Power Combined	4.5-10	36-39.5[1]	14-29
[95]	FC-AlN	Resistive/Reactive	6.5-18	32.6-34.3[2]	13-39

[1]Saturated Power (P_{SAT}), [2]3-dB Compression (P_{3dB}), [3]1-dB Compression, (P_{1dB})
Hybrid implementations: **WB-ML**: Wire-bond on multilayer board, **WB-C**: Wire-bonded on ceramic (unspecified type), **FC-AlN**: Flip-chip on AlN.

same package platform [104,105]. The traditional approach to multilayer packaging for microwave applications started with the use of high-temperature co-fired ceramics (HTCCs), in which alumina (Al_2O_3) sheets are bonded together through a high temperature (~1500 °C) firing step. Using such a high temperature poses two problems. Firstly, lower cost and conventionally used microfabrication metals (e.g., aluminum or copper) are precluded from use since they have lower melting temperatures (i.e., 962°C-1085°C). This makes it necessary to use alternative conductors, such as molybdenum or tungsten, whose conductivities are lower and therefore introduce significantly increased conductor loss as the frequency increases. Secondly, the high temperature also does not permit chip embedding for true 3D integration. To address these issues, low-temperature co-fired ceramics, or LTCCs, which can be bonded within the 850-900 °C temperature range were adopted next. LTCCs are composed of a combination of alumina with glass. Since their introduction, much work has been done to create multi-chip and mm-wave modules [106, 107]. The drawback of LTCCs, however, is that they experience shrinkage during the firing process. In multi-layer designs, this can introduce stresses and reduce reliability.

Beyond ceramics, organic substrates are also heavily used and studied for electronics

Table 1.4. Comparison ceramic and organic packaging substrate materials for high frequency systems-on-package (SOP). [110–113]

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Property	HTCC	LTCC	FR-4	PTFE	LCP
tanδ (at f = 1 GHz)	0.0002	0.0025	0.016-0.055	0.0028	0.004
CTE [ppm/°C]	3.3-7	3-7	13-14	24	3-30
Bond Temperature [ppm/°C]	1450-1880	850-1000	N/A	343	300
ϵ_r	7-10	3.5-9	4.35-4.7	2-2.1	3.15
Moisture Absorption [%]	≃0	≤0.1	≤0.25	≤0.015	≤0.02-0.04
Thermal conductivity [$\mathrm{W\,m^{-1}\,K^{-1}}$]	17	2-4	0.3	0.5-0.95	0.2

packaging. FR4, a glass-woven epoxy, is perhaps the best known example and is very popular for printed circuit boards. Polytetrafluoroethylene (PTFE), and its composites, as well as liquid crystal polymner (LCP) are further examples of organic substrates that have been used for higher frequency applications. LCP has the advantage of being flexible, can be produced in large area thin sheets (i.e., 25-100 μm per sheet), and has been characterized to offer low loss up to 170 GHz [108, 109].

Table 1.4 offers a comparison of the above mentioned organic and ceramic materials for SOP applications. It can be concluded that organics, particularly LCP, offer similar radio-frequency characteristics (i.e., low loss) as ceramics, with the benefit of lower bonding temperature, which facilitates chip embedding and 3D integration. Moreover, both PTFE and LCP have lower moisture absorption rates than LTCCs, meaning that they can offer near hermetic performance. The wealth of attractive attributes in organics has driven the demonstration of organic-based modules with CMOS [114], SiGe [115, 116] and GaAs [117] technologies. Due to the thermal management necessary to handle the high-power operation of GaN, organics have been thus far overlooked since they have a low thermal conductivity.

1.6 Thesis Objectives

The above review of InGaZnO TFTs and GaN power amplifiers has revealed a number of shortcomings in the current state-of-the-art. These can be summarized as follows:

1. Gas phase chemical sensors that use InGaZnO are either fabricated or operated at high temperatures that are not compatible with low-cost and flexible substrates.

2. Reliable thin film passivation of InGaZnO TFTs remains a challenge, and the critical processing parameters of thin film passivation are not well understood.

3. Double-gate TFTs have thus far relied on high temperature thermal oxide films to achieve Super Nernstian pH sensitivity, and therefore have only been realized on Si substrates.

4. Current packaging methods for GaN devices and circuits use expensive and lossy materials.

5. Hybrid GaN power amplifiers have been predominantly realized using wire-bond interconnects that introduce parasitics and limit bandwidth.

6. Organic laminates offer low loss up to the mm-wave regime, low-cost and can be processed using traditional PCB-based methods. However, their low thermal conductivity thus far ruled out their use for GaN-based systems.

Motivated by these challenges, the overarching objective of this thesis is to leverage low-temperature fabrication techniques to evaluate InGaZnO TFTs as chemical sensors, and develop advanced packaging methodologies that enable hybrid GaN/organic high frequency circuits.

In the context of InGaZnO, a wafer-level microfabrication process for TFTs based on this material has been developed. The maximum thin film deposition temperature is 180°C, with subsequent post-process annealing ranging from 100°C to 300°C. This low thermal

budget has permitted the fabrication of the TFTs on both traditional Si substrates as well as transparent glass, and is also compatible with flexible plastic substrates. Device and thin film characterization techniques are employed to evaluate TFT device performance, and are correlated to the thin film deposition process parameters. The emphasis of development is not placed on optimizing the electrical performance parameters, such as mobility, in these TFTs; rather the focus is on understanding and improving their viability for chemical sensor deployment. Thus, key metrics include bias stress stability, sensitivity, and reliability of operation in a liquid environment where applicable. Bias stress stability is improved using three methods: 1) post-process annealing, 2) pulse-mode biasing and 3) thin film passivation. Sensing of gas-phase ethanol, a volatile organic compound (VOC), is demonstrated with InGaZnO TFTs at room temperature for the first time. The sensitivity of these sensors is improved by introducing an insulating polymer capping layer. To enable liquid-phase operation and sensing, atomic layer deposition (ALD) is leveraged as it permits low temperature deposition of high-ϵ_r dielectrics. The deposition temperature dependent characteristics of TiO_x passivated TFTs is analyzed, suggesting that oxygen gettering affects performance. This scheme is then deployed to develop dual-gate TFTs with pH sensitivity beyond the Nernst Limit. Moreover, these devices are fabricated with a maximum process temperature of 180°C and can therefore be made on flexible substrates in the future. Lastly, an alternative and novel application of InGaZnO TFTs for biochemical liquid sensing is explored that alleviates the need for the vacuum-based passivation of InGaZnO discussed above. Namely, a two-stage Zn ion sensor is demonstrated on a glass substrate using a photoluminescent sensing polymer, TPN-Cl_2, and a InGaZnO/PQT-12 based phototransistor.

The development of hybrid GaN/organic high power PAs is pursued through the development of thermal packaging and microwave circuit design. Due to its excellent low-loss characteristics, low-cost and near hermeticity, LCP is chosen as the organic packaging laminate for this study. Firstly, the limitations of applying traditional wire-bond and flip-chip bond packaging strategies to GaN on LCP are evaluated and compared against the use of a

high thermal conductivity ceramic, aluminum nitride (AlN). This is achieved by employing infrared (IR) temperature metrology, and analyzing the effects of self-heating on the pulsed I-V characteristics. It is found that wire-bonded 6 W GaN HEMTs on LCP can only be operated up to 10% duty cycle, whereas flip-chip bonded devices on LCP must be operated below 1% duty cycle. Given these results, a novel packaging scheme that permits flip-chip bonding and device encapsulation within a multi-layer organic stack-up is proposed. This package minimizes interconnect parasitics compared to traditional wire-bonded packages, thereby facilitating the design of wideband amplifiers and RF systems. Pulsed and CW I-V characterization confirm reliable thermal performance. Finite element modeling, in conjunction with large signal simulations, are exploited to design a hybrid power amplifier with this package that operates in the X-Band. Characterization of the fabricated module reveals 5.4 W output power, the largest power achieved so far by any flip-chip bonded GaN/organic PA. Lastly, the developed techniques for encapsulated packaging in organics are applied to heterogeneous semiconductor chips with mixed interconnect strategies. Resulting from this work is the widest bandwidth hybrid receiver on organics. Together, these technologies can be used to create high performance heterogeneous systems on organics.

1.7 Thesis Outline

To address these research objectives, this thesis is outlined in the following manner:

Chapter 2 provides an introduction into the design and operation of thin film transistors (TFTs). The electrical characteristics of these devices is described, along with methods to extract key metrics.

Chapter 3 describes the low-temperature microfabrication processes that have been developed to manufacture InGaZnO TFTs. Current-voltage (I-V) measurements of the fabricated devices are provided, along with characterization of the thin films themselves.

Chapter 4 presents two schemes to improve bias stress stability: post-fabrication annealing and pulsed-mode operation. The improved bias stability is then leveraged to demonstrate gas sensing of ethanol. By capping the bare InGaZnO TFTs with an insulating polymer layer, it is also shown that chemical sensitivity can be enhanced.

Chapter 5 studies methods for the passivation of InGaZnO using inorganic thin films. Passivation is essential for both further improving bias stress stability beyond the two methods presented in Chapter 4, as well as to permit the operation of InGaZnO in a liquid media for pH sensing. Among the investigated passivation strategies, it is found that ALD TiO_x is a promising candidate, and results are presented regarding the impact of deposition temperature on device performance.

Chapter 6 builds on the passivation results shown in Chapter 5 to create double-gate InGaZnO TFTs with pH sensitivity beyond the Nernst Limit. Microfludic packaging is deployed for the TFTs and reliable performance in liquid is presented.

Chapter 7 investigates the light sensitivity of bottom-irradiated bare InGaZnO TFTs as well as InGaZnO/PQT-12 phototransistors on glass. The enhanced light sensitivity of the phototransistor permits is integration with a photoluminescent and liquid stable sensing polymer to form a novel Zn ion sensor.

Chapter 8 studies the feasibility of traditional packaging techniques (i.e., wire-bonding and flip-chip bonding) on organic and ceramic substrates for GaN transistors. Thermal infrared (IR) measurements are obtained, as well as pulsed I-V characteristics to correlate packaging effects on device performance.

Chapter 9 introduces the first-ever encapsulated GaN/organic package using flip-chip interconnects for wideband performance. The package's thermal performance is evaluated and achieves reliable CW operation. Thereafter, a multi-watt X-Band power amplifier is designed, fabricated and tested.

Chapter 10 presents a technique to heterogeneously integrate wideband MMIC chips within a multilayer organic package. Unique interconnects are used for each chip, which

provides design flexibility and modular development. A receiver is demonstrated using this scheme, which achieves the widest bandwidth among hybrid receivers to date.

Chapter 11 summarizes the achievements and contributions of this work, and outlines avenues of potential future research.

CHAPTER 2

PHYSICS AND OPERATION OF InGaZnO THIN FILM TRANSISTORS

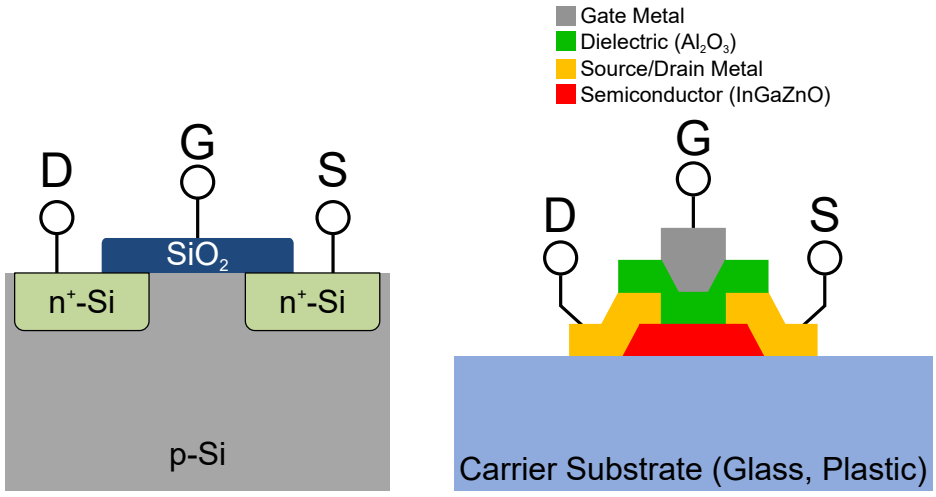
In this chapter, the device structure and fundamental principles that govern the operation of InGaZnO thin film transistors (TFTs) are explained. The generalized current-voltage (I-V) characteristics of n-channel TFTs are derived from first principles. Methods to extract fundamental performance metrics, such as threshold voltage and mobility, from ideal I-V curves are then described. Lastly, background information is provided regarding material properties that are particular to InGaZnO and how they affect device performance.

2.1 Thin Film Transistor Operation

TFTs are a type of field-effect transistor (FET), or voltage-controlled current source. In the following sections, the operation of TFTs is explained. Firstly, the most common TFT structures are presented and a clear distinction is drawn between these devices and the typical silicon-based complementary metal-oxide- semiconductor (CMOS) metal-oxide-semiconductor field effect transistor (MOSFET). A brief overview of the semiconductor physics principles that govern the operation of TFTs is provided. Finally, typical current-voltage (I-V) characteristics are presented, along with explanations of key performance parameters that can be extracted from these curves.

2.1.1 Device Structure

Figure 2.1a depicts the device cross-section of an n-channel Si MOSFET. These devices are fabricated monolithically, meaning that each functional region is formed through the strategic manipulation of the original Si substrate itself. That is, the gate dielectric (SiO_2) is obtained through thermal oxidation of Si and the source/drain wells are created by doping certain regions of the Si substrate to convert them from p-type to n-type. The rapid development of Si-based technology was made possible through two key properties: (1) the



(a) (b)

Figure 2.1. Cross-sectional comparison of (a) n-channel Si MOSFET and (b) thin film transistor.

existence of natively occurring SiO_2 that can be grown with high-quality, and (2) reliable and controllable p- and n-type doping that has facilitated the development of complementary digital logic.

In contrast to the monolithic Si MOSFET, thin film transistors (see Figure 2.1b) are formed through the sequential deposition and patterning of separate thin films of mixed materials. As a result, various substrates that are insulating in nature can be selected as a platform to build the TFT on. Common examples of substrates include transparent glass, often used in the flat panel display industry, or plastic, which has gained much popularity in recent years for flexible or wearable low-cost electronics. A semiconductor is first deposited, such as n-type metal oxides (e.g., InGaZnO or ZnO) or p-type organic materials (e.g., pentacene). Source (S) and drain (D) electrodes are formed through a first metal layer deposition, such as chrome/gold (Cr/Au). This is followed by the deposition of a dielectric material, such as SiO_2, SiN_x or Al_2O_3, which forms the gate insulator. Finally the gate electrode is realized via a second metal layer deposition, such as aluminum (Al). In this way, each thin film is formed by different materials, and can be deposited using a wide variety of deposition methods.

To illustrate the differences between TFTs and Si MOSFETs, the TFT in Figure 2.1b

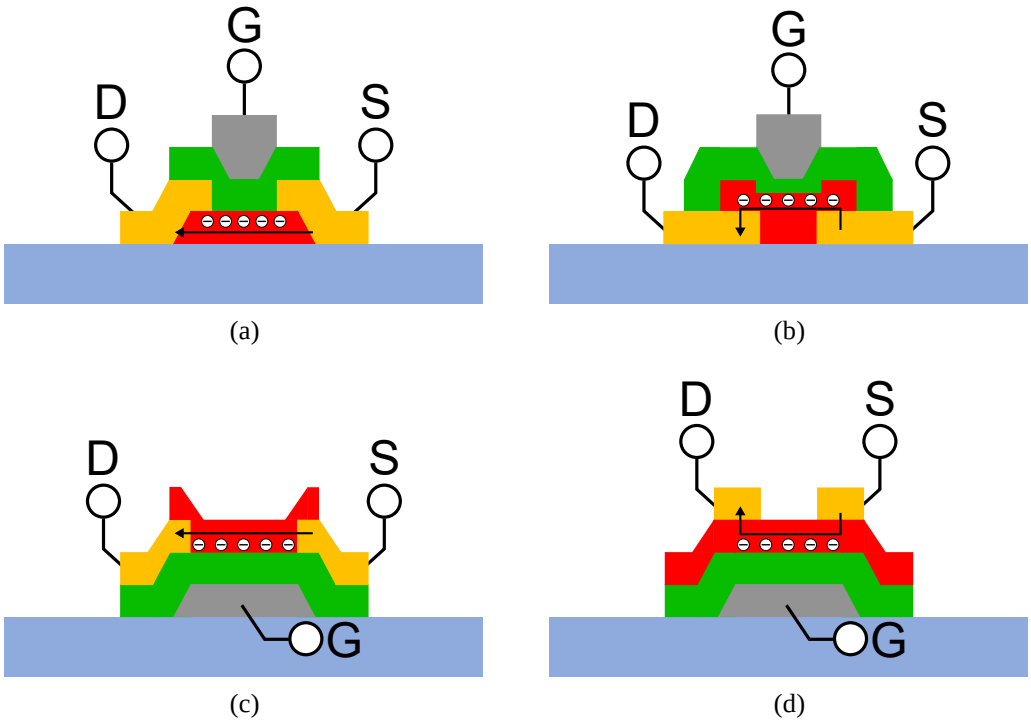


Figure 2.2. Four TFT device structures: (a) Top-Gated/Coplanar, (b) Top-Gated/Staggered, (c) Bottom-Gated/Coplanar, (d) Bottom-Gated/Staggered.

was drawn in a top-gate configuration. However, there exist additional TFT structures, as shown in Figure 2.2 [41, 118, 119]. In general, a TFT's structure is determined by the order in which each of the thin film layers is deposited, which will result in two main architectures: (1) the location of the gate (i.e., top or bottom) and (2) the location of the S/D contacts with respect to the plane of the conducting channel (i.e., coplanar or staggered). Figure 2.2a represents a top-gate, coplanar TFT. It is observed that the conducting channel's plane intersects with the S/D contacts and therefore electrons/holes flow horizontally across. In Figure 2.2b, however, the channel lies slightly above the top of the boundary of the S/D contacts, therefore making this configuration a top-gate, staggered TFT. Similar rationale can be applied to define the devices in Figures 2.2c and 2.2d, which are both bottom-gate devices with co-planar and staggered S/D contacts, respectively. In this work, the TFTs are fabricated in a bottom-gate, staggered configuration due to their ease of fabrication and compatibility with industrial TFT processes used for flat panel products [120].

2.1.2 Metal-Insulator-Semiconductor (MIS) Capacitor Behavior

The theory of TFT operation can, in large part, be represented by the same solid-state semiconductor physics on which the Si MOSFET relies. At the core of the TFT lies a metal-insulator-semiconductor (MIS) capacitor formed by the gate metal, the gate dielectric and the semiconductor thin film layer. Figure 2.3 depicts how variation of the applied voltage across the structure affects energy band bending in the MIS structure with an n-type semiconductor, such as InGaZnO. For the sake of simplicity, it is assumed that this structure is ideal, in that (1) the work function of the metal (Φ_m) and the work function of the semiconductor (Φ_s) are equal to each other and (2) there are no mobile charge traps at the semiconductor-insulator interface.

At equilibrium, there is no voltage applied across the capacitor (V_{GS}=0V) so the metal's Fermi energy ($E_{F,m}$) and the semiconductor's Fermi energy ($E_{F,s}$) lie flat and align (Figure 2.3a). The n-type nature of the semiconductor determines that $E_{F,s} > E_i$. When a negative voltage is applied to the metal with respect to the semiconductor, as shown in Figure 2.3b ($V_{GS} < 0$V), the energy bands of the semiconductor bend upward at the semiconductor-insulator interface and electrons are pushed away. As a result, a non-conductive depletion region is formed. When $V_{GS} > 0$V is applied (Figure 2.3c), electrons are attracted towards the interface and accumulate to create a conductive channel. Whereas Si MOSFETs possess a further regime, in which applying a large enough negative voltage would result in inversion of the semiconductor from n-type to p-type, this type of behavior has not yet been observed in metal oxide semiconductors, such as ZnO and InGaZnO [121, 122]. In summary, a metal oxide TFT's ON state is achieved via accumulation, and is turned OFF via depletion.

2.1.3 TFT Current-Voltage Characteristics

With the fundamental MIS capacitor explained, it is now possible to begin deriving the current-voltage (I-V) characteristics for an n-type TFT. This is carried out by using the long channel approximation often applied to MOSFET devices [123]. Since current density is

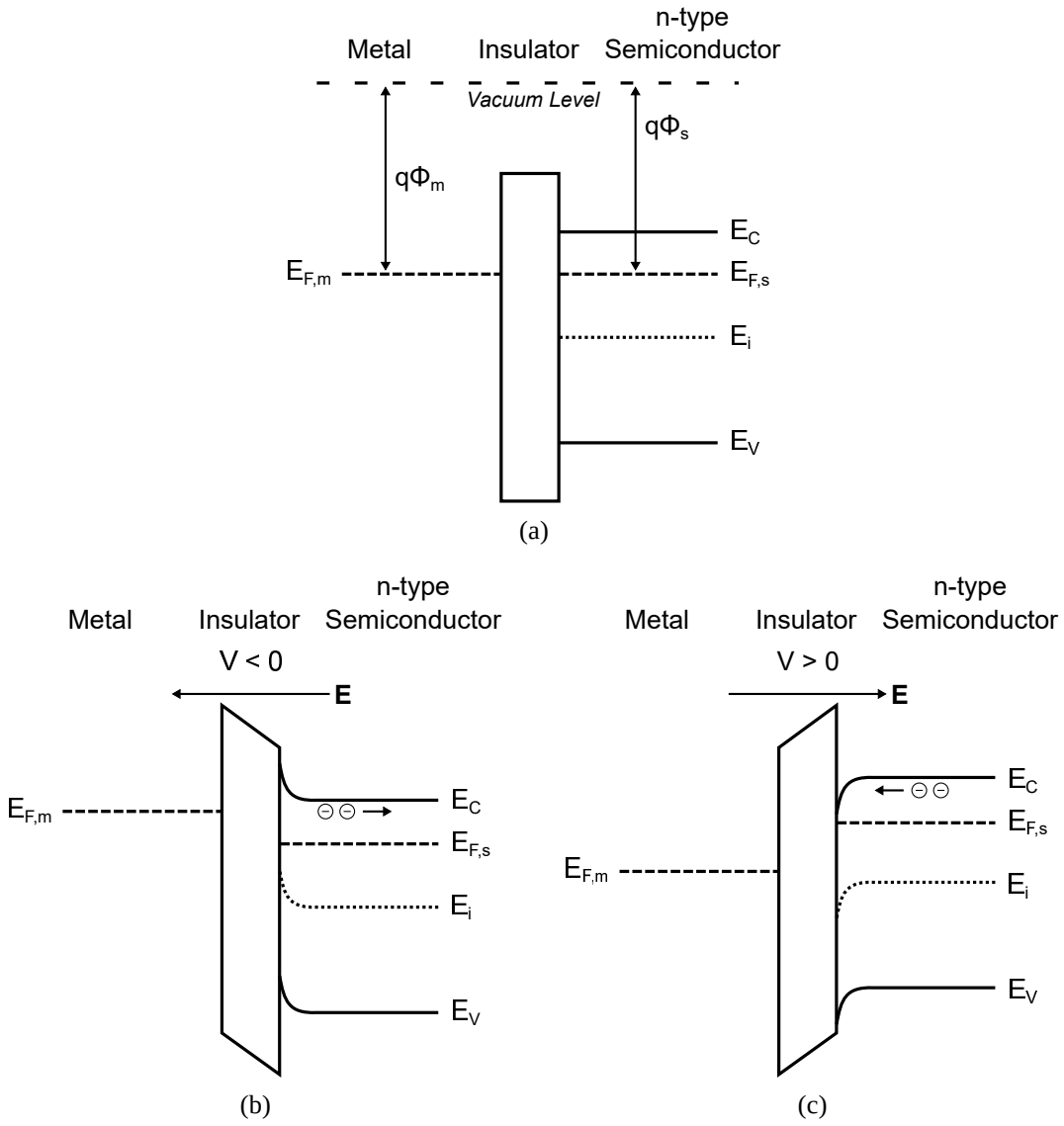


Figure 2.3. Energy band diagrams depicting the three regimes of operation for MIS structure in n-type TFTs: (a) Equilibrium ($V_{GS} = 0V$), (b) Depletion ($V_{GS} < 0V$), and (c) Accumulation ($V_{GS} > 0V$).

defined as the amount of charge passing through a given area per time, the charge induced within the semiconductor channel as a result of the bias applied to the MIS capacitor is first examined. It is well known that:

$$C = \frac{\epsilon_0 \epsilon_r A}{t_i} = \frac{dQ}{dV} \tag{2.1}$$

where C is capacitance, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the insulator material, A is the area of the capacitor, t_i is the thickness of the insulating

film, Q is the balanced charge built up on either plate of the capacitor and V is the voltage applied across the capacitor. The capacitance can then be normalized with respect to the area, giving C_i':

$$C_i' = \frac{C}{A} = \frac{\epsilon_i}{t_i} \tag{2.2}$$

where $\epsilon_i = \epsilon_0 \epsilon_r$. Using the second half of Equation 2.1, a relationship can be established between the charge per unit area in the channel, Q_{ch}', and the gate-source voltage (V_{GS}):

$$C_i' = -\frac{dQ_{ch}'}{dV} = -\frac{Q_{ch}'(V_{GS}) - Q_{ch}'(V_{TH})}{V_{GS} - V_{TH}} \tag{2.3}$$

where V_{TH} represents the threshold voltage, or the voltage at which accumulation occurs in the semiconductor channel. To simplify the model further, it is assumed that when $V_{GS} \leq V_{TH}$, ideal depletion occurs, meaning that $Q_{ch}'(V_{GS} \leq V_{TH}) = 0$ and $I_D(V_{GS} \leq V_{TH}) = 0$. Thus,

$$C_i' = -\frac{Q_{ch}'(V_{GS})}{V_{GS} - V_{TH}} \tag{2.4}$$

and

$$Q_{ch}' = -C_i' (V_{GS} - V_{TH}) \tag{2.5}$$

These equations describe the capacitor in isolation, however in a full TFT an additional bias voltage will be applied between the source and drain nodes (V_{DS}). The voltage that is experienced in the channel as a result of this bias can be expressed as $V_{ch}(x)$. It is a function of the horizontal (x-direction) position along the length of the channel and therefore also affects Q_{ch}':

$$Q_{ch}' = -C_i' (V_{GS} - V_{TH} - V_{ch}(x)) \tag{2.6}$$

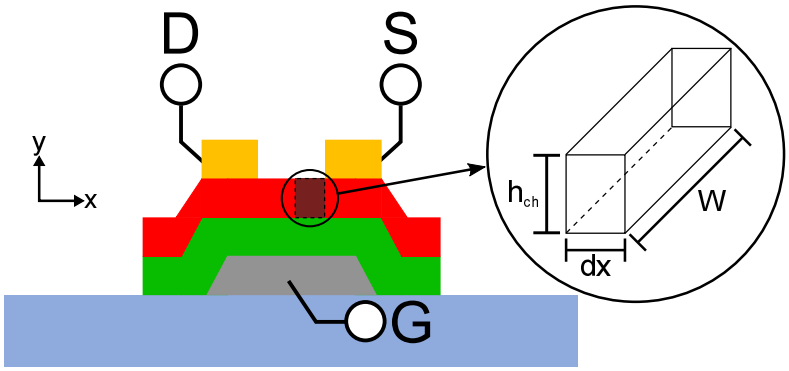


Figure 2.4. Cross-sectional volumetric slice of semiconductor channel.

To correlate Equation 2.6 to the current, the problem needs to be looked at from a slightly different perspective. Figure 2.4 shows a volumetric slice of the channel with thickness h_{ch}, length dx and depth W. Within this volume, the carrier concentration (i.e., number of electrons per unit volume) is given by $n = n(x, y)$. From here, the charge per unit area along the channel, $Q'_{ch}(x)$, is found by taking the integral along the y-direction:

$$Q'_{ch}(x) = -q \int_0^{h_{ch}} n(x, y)\, \mathrm{d}y = -qn_{ind}(x) \tag{2.7}$$

where q is the change of a single electron and n_{ind} is the number of carrier per unit area that are induced in the channel due to accumulation. Subsequently, the drain current (I_D) is related to this charge through the electron velocity $v(y)$ by the expression:

$$I_D = -WQ'_{ch}(x)v(x) = WQ'_{ch}(x)\mu(x)\mathscr{E}_L(x) \tag{2.8}$$

where $\mu(x)$ is the electron mobility and $\mathscr{E}_L(x)$ is the longitudinal electric field strength. To obtain the relationship between V_{DS} and I_D, it is recognized that $\mathscr{E}_L = -\frac{dV_{ch}}{dx}$. Then, this expression can be integrated:

$$\int_0^L I_D\, \mathrm{dx} = \int_0^{V_{DS}} -WQ'_{ch}(x)\mu(x)\, \mathrm{d}V_{ch} \tag{2.9}$$

To solve this integral, it is assumed that both the drain current, I_D, and the mobility, μ, are constant across the length of the channel. Then, equation 2.6 can be substituted into

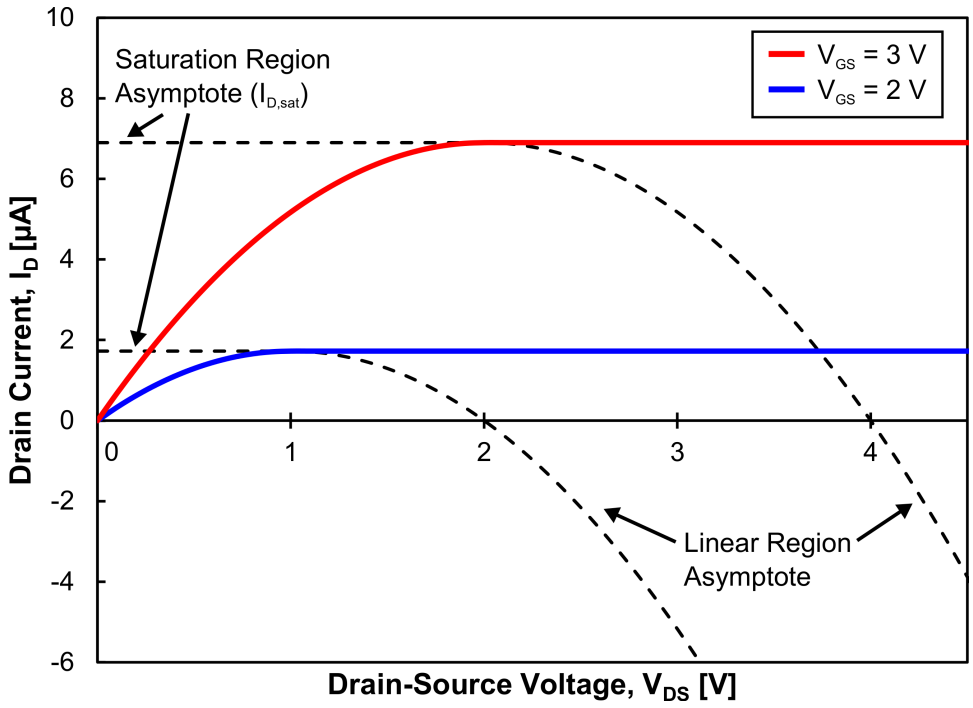


Figure 2.5. $I_D - V_{DS}$ **plot using theoretical equations.**

equation 2.9:

$$I_D \int_0^L \mathrm{dx} = -W\mu \int_0^{V_{DS}} -C_i' \left(V_{GS} - V_{TH} - V_{ch}\right) \mathrm{d}V_{ch} \tag{2.10}$$

$$I_D = \frac{WC_i'\mu}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{2.11}$$

The $I_D - V_{DS}$ characteristic based on equation 2.11 is plotted in Figure 2.5 for two different values of V_{GS}. The parabolic nature of the curves implies that there is a maximum I_D, followed by a monotonic decrease, extending to the negative range. Clearly, this equation does not fully describe a TFT on its own. To understand where the limitations come from, equation 2.6 must be considered in more detail. It is evident that at the source contact $V_{ch}(0) = V_S = 0$, and therefore always obeys $V_{GS} - V_{TH} > V_{ch}$ when the device is turned on. Likewise, at the drain end of the channel, $V_{ch}(L) = V_{DS}$. At this point, if $V_{DS} > V_{GS} - V_{TH}$, then $Q_{ch}'(L)$ becomes positive, which implies that holes dominate the channel. As stated above, this is not possible. This hints that there must exist two regions of operation: the

linear/triode region, and the saturation region. Equation 2.11 describes the behavior of the TFT in the linear region, where $V_{DS} < V_{GS} - V_{TH}$.

The saturation region is bound at the lower end by

$$V_{DS,sat} = V_{GS} - V_{TH} \tag{2.12}$$

The points that satisfy Equation 2.12 are also known as the pinch-off points. Substituting $V_{DS,sat}$ for V_{DS} into equation 2.11, it becomes:

$$I_D = I_{D,sat} = \frac{WC_i'\mu}{L}\left[(V_{GS} - V_{TH})V_{DS,sat} - \frac{V_{DS,sat}^2}{2}\right] \tag{2.13}$$

$$I_{D,sat} = \frac{WC_i'\mu}{2L}(V_{GS} - V_{TH})^2 \tag{2.14}$$

It is important to notice that equation 2.14 is now independent of V_{DS}, as we would expect. All in all, equations 2.11 and 2.14 provide a first-order approximation of the behavior of TFTs in the linear and saturation regions, respectively. As mentioned above, several assumptions have been made that do not capture some real effects observed in practice (e.g., constant mobility and contact resistance), but the equations can still be used to illustrate the fundamental operation of the device.

2.1.4 Physical Representation of Device Operation

In order to understand the implications of the above-derived equations, the distribution of charge in the TFT channel is shown in Figures 2.6a-2.6d for different bias conditions, and linked to the I-V curves in Figure 2.6e. In the ideal OFF-state ($V_{GS} < V_{TH}$), there are no free charges in the device's channel to conduct current (Figure 2.6a). The TFT therefore acts as an open-circuit under ideal conditions or, in practice, a high resistance resistor between the drain and source terminals. Once a large enough voltage bias is applied to the gate terminal in order to accumulate charge in the channel ($V_{GS} > V_{TH}$), current can flow. While $V_{DS} << V_{GS} - V_{TH}$ (i.e., V_{DS} is small enough so that the V_{DS}^2 term in Equation 2.11

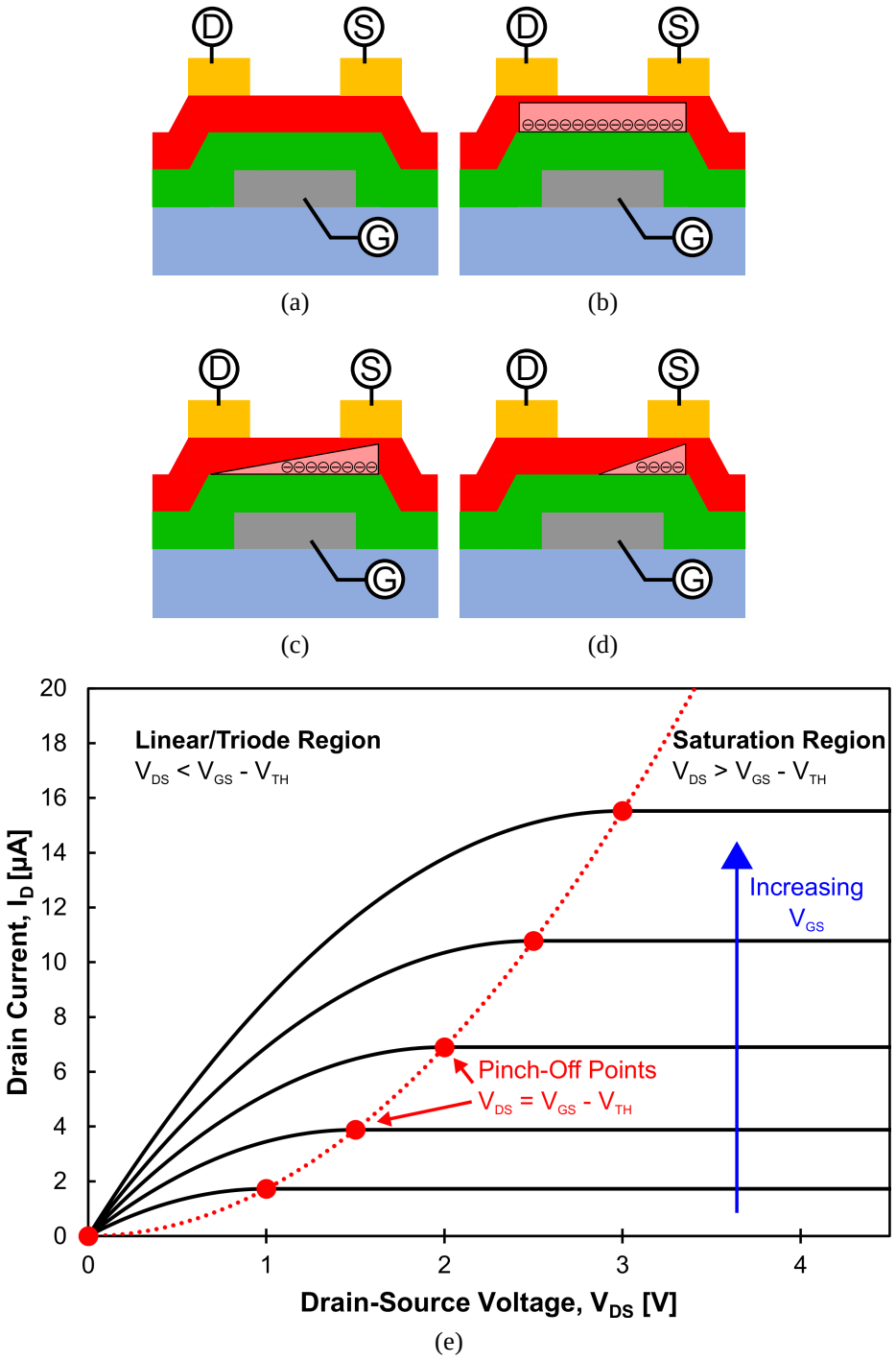


Figure 2.6. Cross-sectional view of a bottom-gate staggered TFT indicating the distribution of charge carriers in the channel in the (a) off state ($V_{GS} < V_{TH}$), (b) in the linear region ($V_{GS} > V_{TH}$ & $V_{DS} < V_{GS} - V_{TH}$), (c) at pinch-off ($V_{GS} > V_{TH}$ & $V_{DS} = V_{GS} - V_{TH}$) and (d) in the saturation region ($V_{GS} > V_{TH}$ & $V_{DS} > V_{GS} - V_{TH}$). (e) Depicts the $I_D - V_{DS}$ output characteristic for multiple values of V_{GS}, while labeling regions of operation that correspond to (a)-(d).

can be ignored), the relationship between I_D and V_{DS} is linear, effectively making the TFT a V_{GS}-controlled resistor (Figure 2.6b). The linear I-V relationship ceases to hold when $V_{DS} = V_{GS} - V_{TH}$ (Figure 2.6c), causing I_D to saturate. This is called the "Pinch-Off" point. As V_{DS} is increased further within the saturation mode (Figure 2.6d), electrons arriving to the end of the accumulation region are swept across the depleted channel area due to the large electric field.

2.2 Parameter Extraction

The above discussion has shed light on the general operation of TFTs. In practice, the development of new materials and fabrication processes for these devices requires the experimental verification and characterization of their performance. This can be achieved, in large part, by extracting parameters, such as the mobility and threshold voltage, from the I-V measurements that are collected. Figure 2.6e represents the output characteristic ($I_D - V_{DS}$) of a TFT, which can be useful to distinguish the triode region from the saturation region to a first order. Moreover, observation of a linear $I_D - V_{DS}$ slope in the triode region confirms the formation of an ohmic contact between the S/D metalization and the semiconductor, as opposed to a Schottky contact that would manifest itself in the form of an exponential rise in current [124].

An alternative I-V measurement involves sweeping V_{GS} for a constant V_{DS}. The resultant $I_D - V_{GS}$ curve is known as the transfer characteristic, and is shown in Figure 2.7 in two forms. The first is to plot $\log_{10} I_D$ on the y-axis (Figure 2.7a). Doing so unveils the switch-like behavior of TFTs in the form of two distinct states of operation: one where there is low current ("OFF" state) and another where there is high current ("ON" state). Quantitatively, this can be represented by the on/off ratio:

$$\text{On/Off Ratio} = \frac{I_{ON}}{I_{OFF}}[\text{unitless}] \tag{2.15}$$

where an ideal TFT possesses an on/off ratio of infinity. In the following sections, the

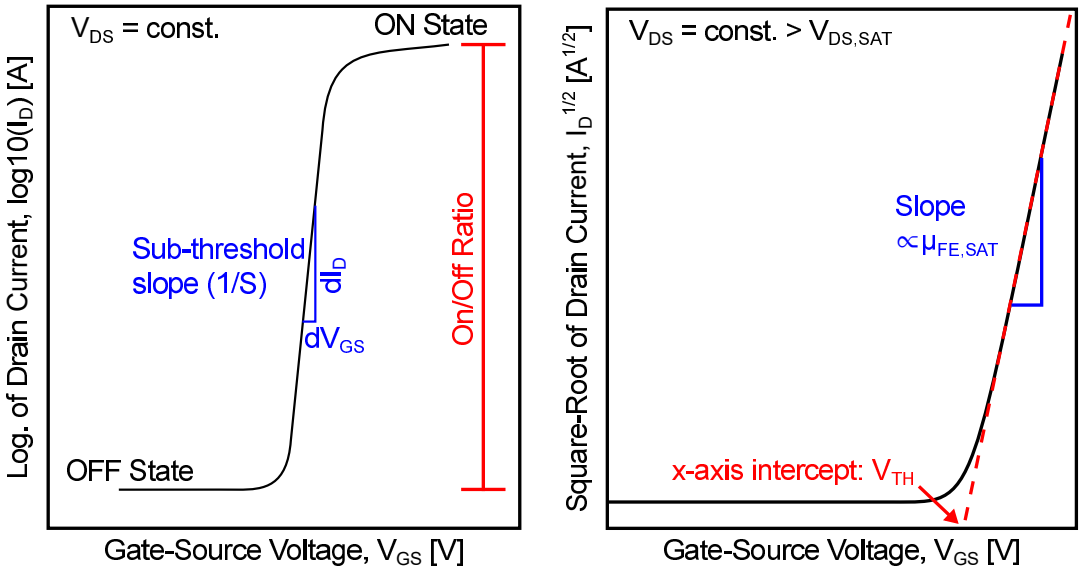


Figure 2.7. Transfer characteristic of a TFT expressed as (a) $\log_{10}(I_D) - V_{GS}$ **and (b)** $sqrt(I_D) - V_{GS}$**.**

process to extract further parameters from these curves will be described.

2.2.1 Sub-threshold Swing

The sub-threshold slope ($\frac{d\log_{10} I_D}{dV_{GS}}$) describes the steepness of the transition from the off to the on state. Ideally, this value also tends to infinity. In practice, in stead of reporting the sub-threshold slope, device engineers prefer to report the sub-threshold swing (S), which is the inverse of the slope:

$$\text{Sub-threshold Swing, S} = \frac{dV_{GS}}{d\log_{10} I_D}[\text{mV/dec}] \tag{2.16}$$

In this way, S gives an idea of how much of a V_{GS} increase is required to obtain an order of magnitude increase in I_D. For a TFT, S yields insight into the magnitude and quality of the device's capacitances:

$$\text{S} = \frac{k_B T}{q}\left(1 + \frac{C_d + C_{ss}}{C_i}\right)\ln 10 \tag{2.17}$$

where $\frac{k_B T}{q}$ represents a voltage contribution from the temperature and is composed of the Boltzmann constant ($k_B \approx 1.38\text{x}10^{-23}$ J K^{-1}), temperature (T) and charge (q). Meanwhile,

C_d is the depletion layer capacitance and C_{ss} is the capacitance that represents the number of charge-filled interface states. These capacitors arise from the MIS capacitor model in Figure 2.3. In order to minimize S, therefore, it is important to minimize C_d and C_{ss}, while maximizing C_i, the gate insulator capacitance. C_{ss} can be reduced by forming a high quality dielectric-semiconductor interface with a small number of interface states, while C_i can be increased through the use of dielectric materials with high ϵ_r. For the purpose of benchmarking, it should be noted that at room temperature (T = 300 K), an ideal device will exhibit an $S = (k_B T/q) \times \ln 10 = 60$ mV/dec.

2.2.2 Threshold Voltage

The threshold voltage, V_{TH}, is a critical indicator of device behavior. For n-channel devices, $V_{TH} > 0V$ describes an enhancement-mode device, implying that a conducting channel is not inherently present. This type of operation is preferred for low-power circuits and applications. Depletion-mode TFTs, where $V_{TH} < 0V$, can also be fabricated. Despite the major importance of V_{TH}, its definition is not consistent across the literary landscape, making it important, therefore, to explicitly identify what definition is being used for each work.

In this work, unless otherwise stated, V_{TH} is obtained by examining the square root of the drain current, or $\sqrt{I_D} - V_{GS}$, with a large enough value of V_{DS} such that the device is operated in the saturation region, as shown in Figure 2.7b. From equation 2.14, this yields a linear relationship:

$$\sqrt{I_{D,sat}} = \sqrt{\frac{WC_i'\mu}{2L}}(V_{GS} - V_{TH}) \tag{2.18}$$

where V_{TH} can be extracted as the x-axis intercept:

$$V_{TH} = V_{GS}\Big|_{I_{D,SAT}=0} \tag{2.19}$$

2.2.3 Field-Effect Mobility

The mobility plays a pivotal role in determining the performance a TFT. As described in Table 1.2, one of the reasons that InGaZnO has gained so much interest is because its mobility is larger than what has been observed in competing low-temperature semiconductors used for TFTs, such as organic semiconductors and a-Si. This permits smaller devices to be produced while maintaining relatively large currents for driving OLEDs. Moreover, the higher the mobility, the higher the switching frequency the TFTs can be operated with. The transfer ($I_D - V_{GS}$) characteristic can be leveraged once again to determine the field-effect mobility, μ_{FE}. It should be noted that this mobility is, in fact, often different in value from the mobility that is measured with other experimental means, such as Hall measurements. This is because carriers in a TFT are transported in response to an electric field, which is determined by the voltages applied to the device, as well as the capacitances. Moreover, coulomb scattering events can occur at the dielectric-semiconductor interface which may reduce the mobility compared to the case within a pristine thin film [125].

When the device is operated in the linear region, the linear field-effect mobility ($\mu_{FE,lin}$) can be obtained via the transconductance, g_m:

$$g_m = \frac{dI_D}{dV_{GS}}\bigg|_{V_{DS}<V_{GS}-V_{TH}} = \frac{W\mu_{FE,lin}C_iV_{DS}}{L} \tag{2.20}$$

or

$$\mu_{FE,lin} = \frac{\left(\frac{dI_D}{dV_{GS}}\right)}{C_i'\frac{W}{L}V_{DS}}\bigg|_{V_{DS}<<V_{GS}-V_{TH}} \tag{2.21}$$

Thus, the slope of the transfer characteristic, along with the gate capacitance density, device geometry and V_{DS} reveal $\mu_{FE,lin}$. In a similar fashion, the saturation field-effect mobility ($\mu_{FE,SAT}$) can be obtained by using the slope of the $\sqrt{I_D} - V_{GS}$ plot (Figure 2.7b).

$$\frac{d\sqrt{I_D}}{dV_{GS}} = \frac{WC_i'\mu_{FE,SAT}}{2L}\bigg|_{V_{DS}>V_{GS}-V_{TH}} \tag{2.22}$$

or

$$\mu_{FE,SAT} = \frac{2L\left(\frac{d\sqrt{I_D}}{dV_{GS}}\right)^2}{WC_i'} \tag{2.23}$$

2.3 InGaZnO Material Properties

Thus far, the theoretical concepts that have been described apply to n-type TFTs in general and, with slight adjustments to account for the difference in majority carrier charge, can also be used for p-type TFTs. In this section, some of the fundamental material properties pertaining specifically to InGaZnO, which are markedly different than Si, are presented.

2.3.1 Electronic Structure and Carrier Transport

As can be seen from Tables 1.1 and 1.2, the electron mobility in silicon reduces by several orders of magnitude when it is amorphous compared to its pristine crystalline state. This is in contrast to InGaZnO, whose mobility remains largely unchanged whether it is crystalline or amorphous, as shown in Figure 2.8. To understand this, the electronic structure of InGaZnO must be examined. The lattice organization of crystalline $InGaZnO_4$, along with a number of other metal oxides, was successfully identified as being of the $YbFe_2O_4$ type in 1985 [126]. Specifically, it is constructed by the periodic repetition of a unit cell that is composed of the following sequence of layers: InO_2^-, $GaZnO_2^+$, $GaZnO_2^+$, InO_2^-, $GaZnO_2^+$, $GaZnO_2^+$, InO_2^-, $GaZnO_2^+$, $GaZnO_2^+$. A "ball and stick" representation of the lattice is shown in Figure 2.9a, while a HRTEM image that verifies this model is shown in Figure 2.9b.

The ionic nature of these metal oxide species is the reason behind the disparate formation of a bandgap in silicon versus metal oxide semiconductors [127]. In isolation, electrons belonging to an individual silicon atom lie in s and p orbitals ($1s^2 2s^2 2p^6 3s^2 3p^2$). When silicon atoms are brought into proximity with each other, these orbitals undergo hybridization, forming sp^3 orbitals and covalent bonds. As the atoms are brought closer together to form a lattice, these orbitals split into low energy molecular bonding states ($sp^3\sigma$) that define

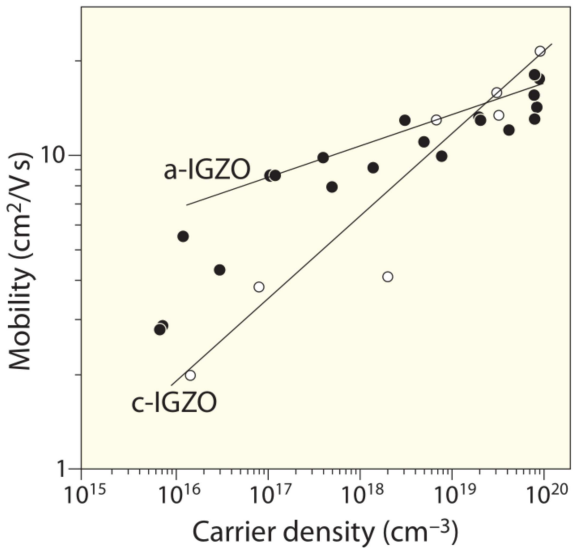
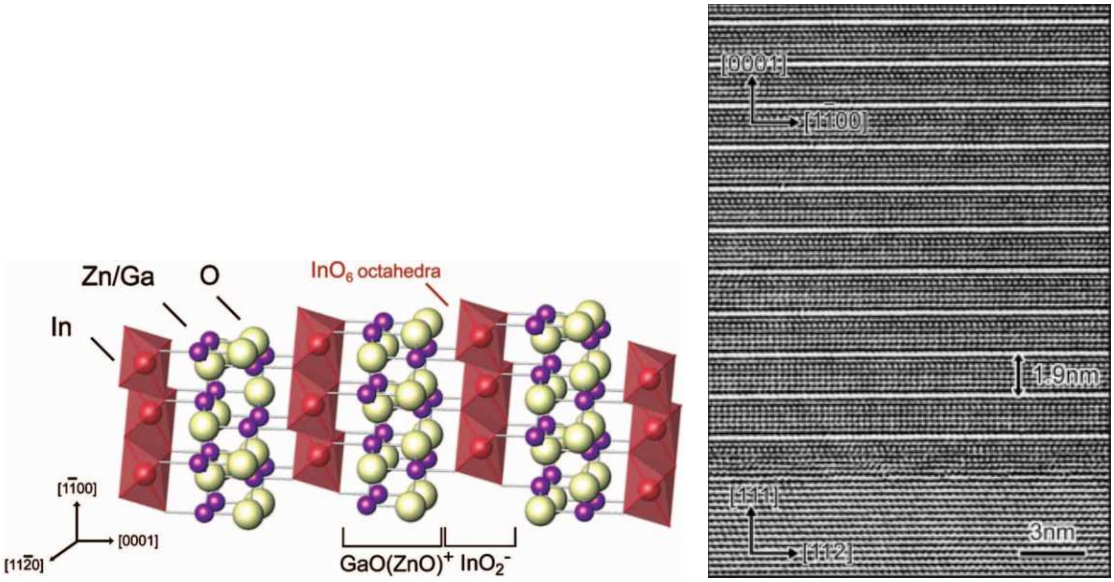


Figure 2.8. Hall mobility comparison between crystalline InGaZnO and amorphous InGaZnO as a function of carrier density [127].



(a) (b)

Figure 2.9. (a) Ball and stick model of crystalline InGaZnO. The InO_2^- layer is composed of In^{3-} ions that form InO_6 octahedra (red polygons). A source of randomness even within this crystal is the distribution of Ga an Zn within the $GaZnO_2^+$ layers. [128] (b) A high resolution transmission electron microscope (HRTEM) image of an IGZO crystal epitaxially grown on a yittria-stabilized zirconia (YSZ) substrate. The repeating unit cell is clearly visible. [129]

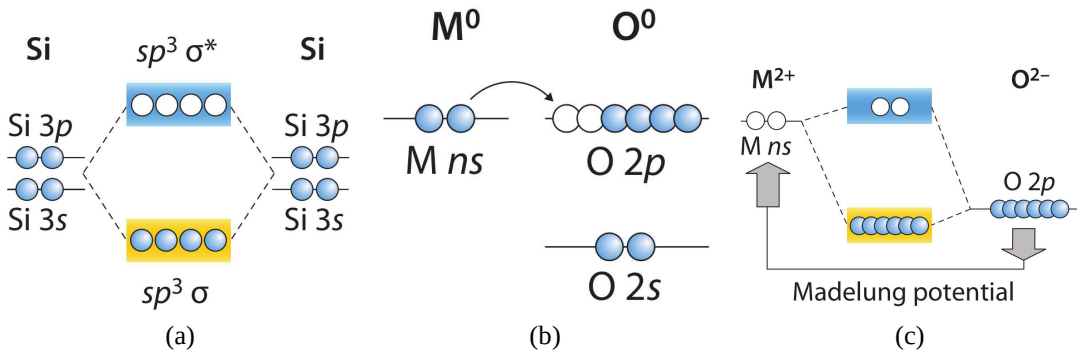


Figure 2.10. Electronic structures of (a) energy bandgap formed in covalent semiconductors, (b) two ionic atoms in close proximity experiencing charge transfer, (c) energy bandgap formed in ionic semiconductors. [127]

the valence band maximum (VBM) and high energy anti-bonding ($sp^3\sigma^*$) states that define the conduction band minimum (CBM), with an energy gap in between (see Figure 2.10a). By contrast, as shown in Figure 2.10b, metals and oxygen start off by existing in a charge-neutral state when in isolation from each other. As a metal and oxygen atom are brought close to each other, the electronegativity of oxygen causes the transfer of an electron from the metal to the oxygen, thus creating a metal cation and oxygen anion. When several ions are collected to form a lattice, there is a balancing of the repulsive and attractive forces. The summation of these electrostatic forces is the Madelung potential. The CBM is thus made up of high energy and unoccupied anion (metal) sites, while the VBM is filled low energy and occupied cation (oxygen) sites (Figure 2.10c).

A three dimensional representation of the CBM, which acts as the carrier transport path, for both types of materials is shown in Figure 2.11. Covalently bonded atoms, such as silicon, are connected via the highly directive sp^3 orbitals. When such a material is made amorphous, the overlap between the orbitals is reduced, leading to localized hopping between tail states. [130] This significantly hampers carrier mobility compared to the crystalline state. As stated above, the CBM in an ionic metal oxide semiconductor is found in the metal, which has large spherical s orbitals. This symmetry dictates that the orientation of neighboring atoms is not as critical, in turn mitigating the reduction in mobility from the crystalline to the amorphous state.

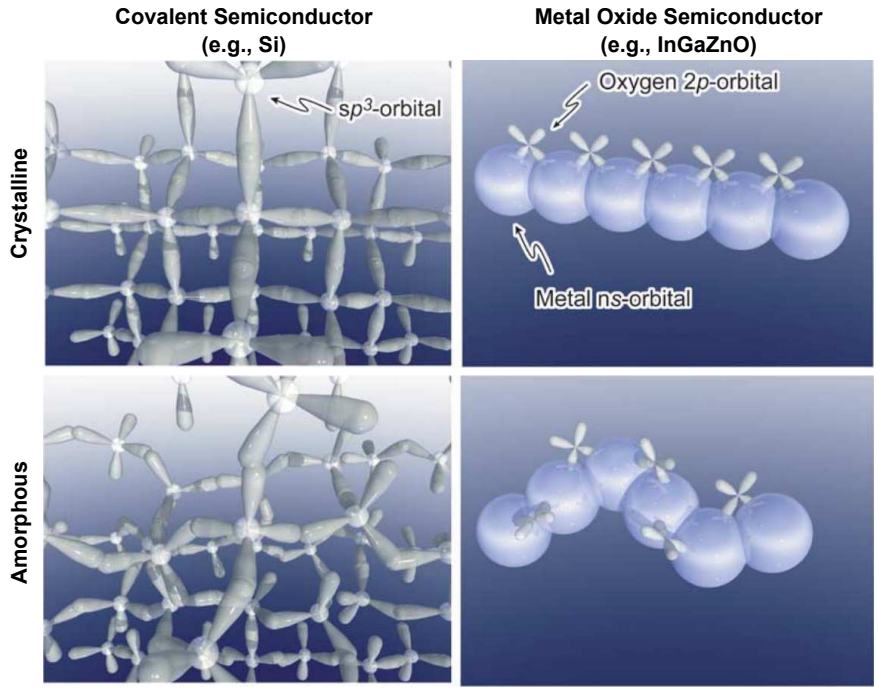
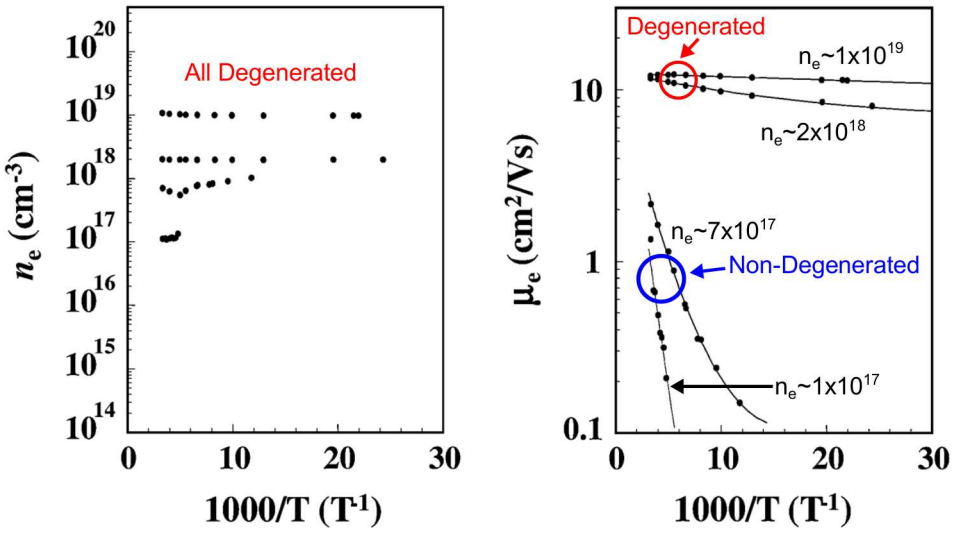


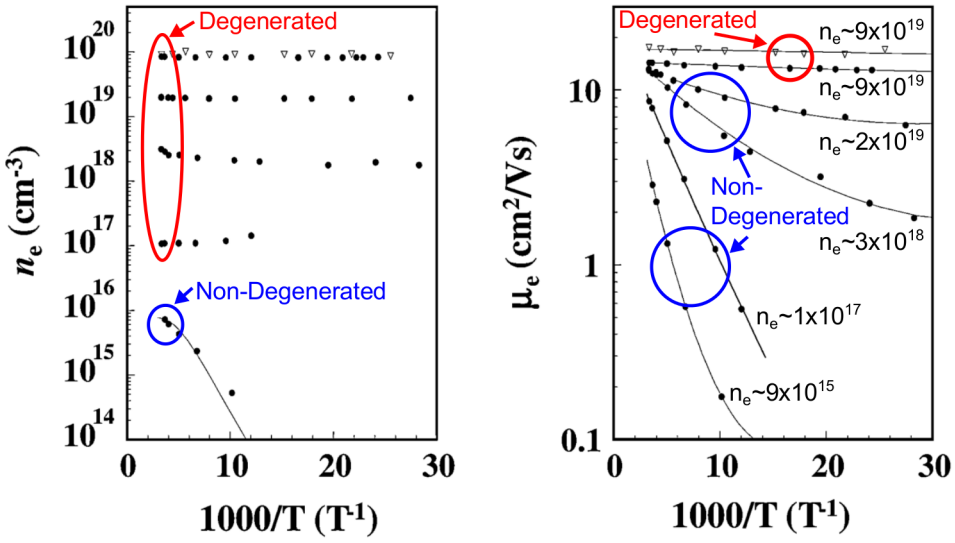
Figure 2.11. Comparison of lattice organization and electron orbitals between covalent and metal oxide semiconductors in both crystalline and amorphous state. [130]

The above models serve to better understand why crystalline and amorphous InGaZnO have similar mobilities, whereas the mobility in Si degrades significantly in its amorphous state. Returning to Figure 2.8, however, it is important to note an additional difference between Si and InGaZnO related to the relationship between mobility and carrier density. In Si, both the hole and electron mobilities fall as the doping/carrier density is increased due to impurity scattering. In InGaZnO, the mobility improves as the carrier density increases. To investigate this unusual effect, temperature dependent studies have been done on both crystalline and amorphous InGaZnO films (Figure 2.12) [131]. The crystalline films were obtained via reactive solid-phase epitaxy (R-SPE) and the doping density was controlled through annealing in a H_2/Ar environment. Pulsed laser deposition (PLD) was used to obtain the amorphous films, where the carrier density was controlled by adjusting the oxygen partial pressure in the chamber.

The electron carrier concentration (n_e) in crystalline InGaZnO (Figure 2.12a) was found to remain stable with temperature when $n_e > 10^{17}$ percm^3, indicating that all of the films



(a)



(b)

Figure 2.12. Carrier concentration (n_e) and Hall mobility (μ_e) versus temperature (T) for (a) crystalline and (b) amorphous InGaZnO. Adapted from [131]

are degenerate. However, Hall mobility measurements revealed that films with $n_e < 10^{18}$ percm^3 were characterized by a temperature-dependent, or non-degenerated, behavior. For the amorphous case (Figure 2.12b), similar results were observed, except that non-degenerated carrier concentrations were found when $n_e < 10^{16}$ cm^{-3}. Moreover, the threshold for degenerated mobility was found to be higher in the amorphous films, in the region of 9x10^{19} percm^3. These results are significant in three ways: (1) they once again confirm that both

crystalline and amorphous InGaZnO behave similarly, (2) they demonstrate that degenerated conduction/mobility can be obtained in amorphous InGaZnO – a behavior that has not been observed in a-Si:H [128] – and (3) they point to the existence of energy barriers above the conduction band edge, since even degenerated carrier concentrations experience non-degenerated mobility.

To explain this phenomenon, a model based on percolation conduction has been proposed [63, 131, 133, 134]. In this model, shown conceptually in Figure 2.13, it is suggested that there exist randomly distributed energy barrier peaks above the mobility edge in the conduction band. As a result, the conduction path of an electron is determined by its energy and its consequent ability to overcome these barriers. Electron path (a), for example, is the shorter and more direct of the two paths shown, and would therefore allow an electron to cross the terrain in the shortest window of time (i.e., highest mobility). Unfortunately, this path is obstructed by high potential barriers that cannot be overcome by low energy electrons. Path (b) circumvents the high barriers, but results in a "windier" and longer path. Below the schematic of the terrain, an energy band diagram explains this in different terms. The Fermi level (E_F) describes the effective energy of an electron, E_{th} describes the threshold energy required to overcome the energy barriers, while E_σ is the activation energy required for an electron to overcome the threshold given its energy, E_F. As the number of

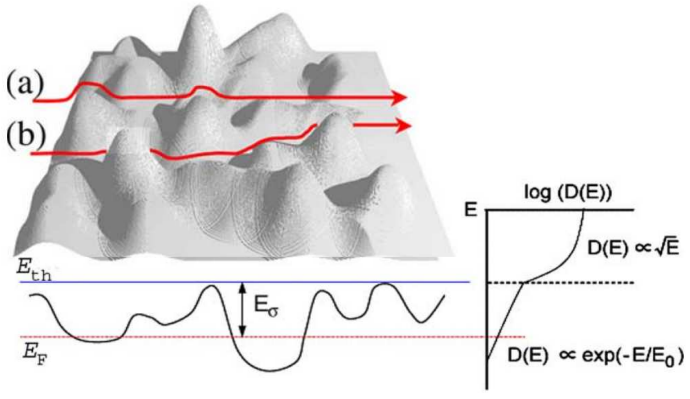


Figure 2.13. Conceptual schematic of the percolation conduction model for carriers in InGaZnO. Adapted from [131, 132].

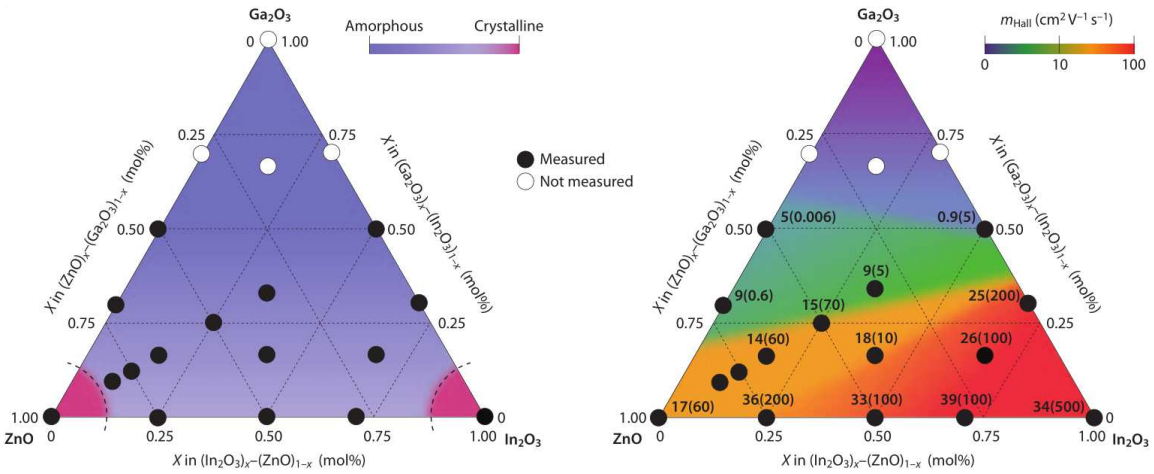


Figure 2.14. Dependence of (left) crystallinity and (right) mobility on the InGaZnO stoichiometry when deposited at room temperature [127].

electrons in InGaZnO increases, E_F rises, lowering the E_σ and increasing mobility. Once E_F reaches or surpasses E_{th}, then degenerate conduction is observed.

2.3.2 Material Composition

Thus far, the stoichiometry of InGaZnO has not been considered. However, it has been found to play an important role in determining both the crystal/amorphous nature of deposited films, as well as their Hall mobility, as presented in Figure 2.14 [127, 135]. Pure metal oxides, such as ZnO, tend to form (poly-)crystalline films rather than amorphous films, even when deposited at room temperature [136]. As binary or tertiary oxides are constructed, amorphous films are achieved. The addition of In increases the mobility, similar to what is seen in other material classes (e.g., ITO or InP). The incorporation of too much In however, makes it difficult to control the electron concentration due to weak In-O bonds that introduce O vacancies and, in turn, free carrier electrons. Ga-O, on the other hand, are stronger than In-O or Zn-O bonds, and therefore serve to stabilize the system. As can be seen in Figure 2.14, too large of a concentration of Ga will also deteriorate the mobility due to the reduction of electrons. This fine balance between the three metal cations is another major reason behind the success of InGaZnO.

CHAPTER 3

LOW-TEMPERATURE FABRICATION AND CHARACTERIZATION OF InGaZnO THIN FILM TRANSISTORS

Building on the fundamental concepts surrounding TFT operation and InGaZnO material properties discussed in Chapter 2, the aim of the work presented in this chapter is to develop a low-temperature and wafer scale microfabrication process for InGaZnO TFTs that can be used for chemical sensing in Chapters 4-6. Therefore, the main focus is not on surpassing the electrical characteristics of state-of-the-art InGaZnO TFTs, but on establishing a robust baseline process for the fabrication of InGaZnO-based (bio-)chemical sensors. The importance of device-level and die-level layout is discussed with respect to their effect on device performance and the feasibility for sensor deployment. Details of the various thin film deposition and lithography process steps are also presented. Thin film characterization techniques are summarized, and the measurement results from these tests are then used in conjunction with electrical I-V characterization of the fabricated TFTs to extract device performance parameters.

3.1 Prior art: InGaZnO TFTs

Some past examples of InGaZnO TFTs were first presented in Section 1.3. The first report of a room-temperature-fabricated InGaZnO TFT was achieved on a flexible PET substrate with a Y_2O_3 gate dielectric and ITO S/D contacts, all deposited with pulsed laser deposition (PLD) [130]. This device exhibited V_{TH} = 1.6 V, $\mu_{FE,SAT}$ = 8.3 $cm^2\,V^{-1}\,s^{-1}$ and an on/off ratio of 10^3. Since then, a number of additional studies have been published, using a wide variety of dielectrics and deposition methods. Due to its reliability, SiO_2 has been used extensively as a gate dielectric, and has been formed either through thermal oxidation (on a Si substrate) [137, 138] or through plasma-enhanced chemical vapor deposition (PECVD) [139, 140]. The former has the advantage of being very reliable, but the disadvantage that

it can only be obtained when using a Si substrate. PECVD allows for the use of alternative substrates, such as glass. High-performance TFTs were obtained on glass using room-temperature radio-frequency (RF) sputtered InGaZnO from a polycrystalline $In_2Ga_2ZnO_7$ target and PECVD SiO_2, with V_{TH} = 5.9 V, $\mu_{FE,SAT}$ = 35.8 $cm^2\ V^{-1}\ s^{-1}$, on/off ratio ~ 5×10^6 and sub-threshold swing of 590 mV/dec [139].

In order to permit low-voltage operation, dielectrics with a large ϵ_r are preferred. Kim et al. reported RF sputtered InGaZnO TFTs with an RF sputtered amorphous BST (a-$Ba_{0.5}Sr_{0.5}TiO_3$) gate dielectric ($\epsilon_r \sim 28$) [141]. These devices showed V_{TH} = 0.5 V, $\mu_{FE,SAT}$ = 10 $cm^2\ V^{-1}\ s^{-1}$, an on/off ratio of 10^7 and sub-threshold swing of 60 mv/dec. A drawback of BST, however, is that the leakage current increases from 10^{-10}A in the OFF region to up to 10^{-6}A in the ON region. Therefore, it is desirable to examine the use of alternative high-ϵ_r gate dielectrics with larger band gaps. A commonly used example is Al_2O_3, which can be deposited using atomic layer deposition (ALD) [142, 143]. For example, ALD Al_2O_3/InGaZnO TFTs have been reported with V_{TH} = 0.4 V, $\mu_{FE,SAT}$ = 8 $cm^2\ V^{-1}\ s^{-1}$, an on/off ratio of 10^7 and sub-threshold swing of 100 mv/dec [142]. Other dielectrics that have been investigated include PECVD SiN_x [144], sputtered PMMA [145], sputtered HfO_2 [146] and electron-beam evaporated $TiO_2/HfO_2/TiO_2$ [147].

3.2 Layout of Sensing Devices and Dies

In Section 2.1.1, four different device structures were presented based on the location of the gate contact (i.e., top or bottom), as well as the vertical position of the semiconductor channel with respect to the S/D contacts (i.e., staggered or coplanar). In this thesis, InGaZnO TFTs are built using a bottom gate, staggered topology. This particular topology was chosen with the application of biochemical sensing in mind. By placing the semiconductor layer at the top-side, the direct interaction between the InGaZnO and chemical analytes can be studied. Moreover, the bias point can be defined independently from the

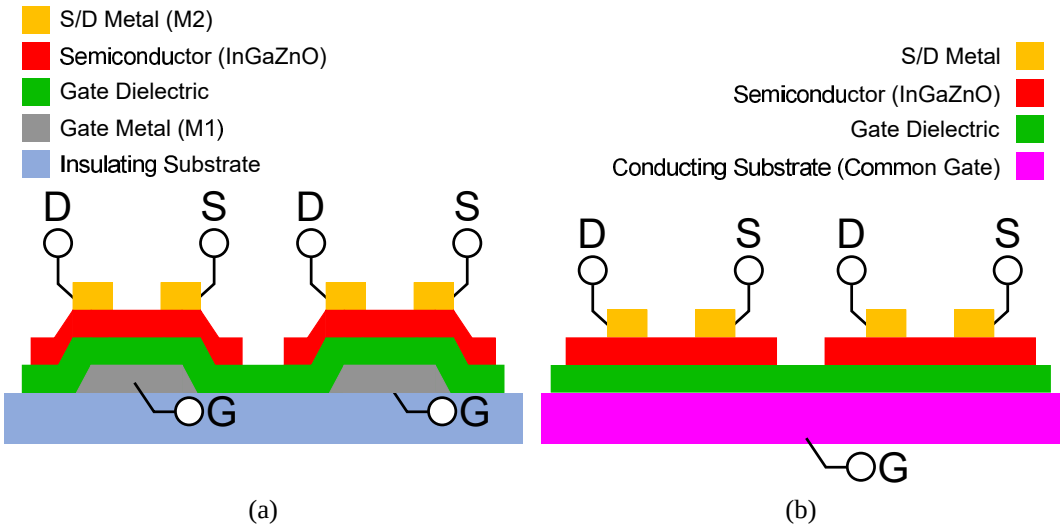


Figure 3.1. Bottom gate, staggered TFTs with (a) individually addressable gate contacts, and (b) common gate contact formed by a conducting substrate.

bottom, opening up the possibility of dual-gate devices (presented in Chapter 6). The staggered configuration dictates that the S/D contacts are formed last, thereby allowing the semiconductor film to be deposited on an unperturbed gate dielectric, which should improve the interface between the two. In addition to the fundamental device structure, the device layout plays an important role in determining the performance of a TFT. The following sections offer an overview of the development of InGaZnO TFT technology studied in this work, showing the changes in device and wafer-level layout that were made along the way to improve electrical performance, provide compatibility with microfluidic packaging techniques and, finally, test structures for thin film characterization.

3.2.1 Generation 1

In Figure 2.2d, the TFTs were conceptually depicted as being fabricated on insulating substrates, such as glass or plastic. However, for the purposes of semiconductor material development, another frequently adopted approach involves using a conducting or semiconducting substrate, such as a highly doped Si wafer, to act as a common gate for all the devices on that sample. The difference between the two approaches is shown in Figure 3.1. The advantages of the common gate strategy are two-fold: (1) less processing is involved

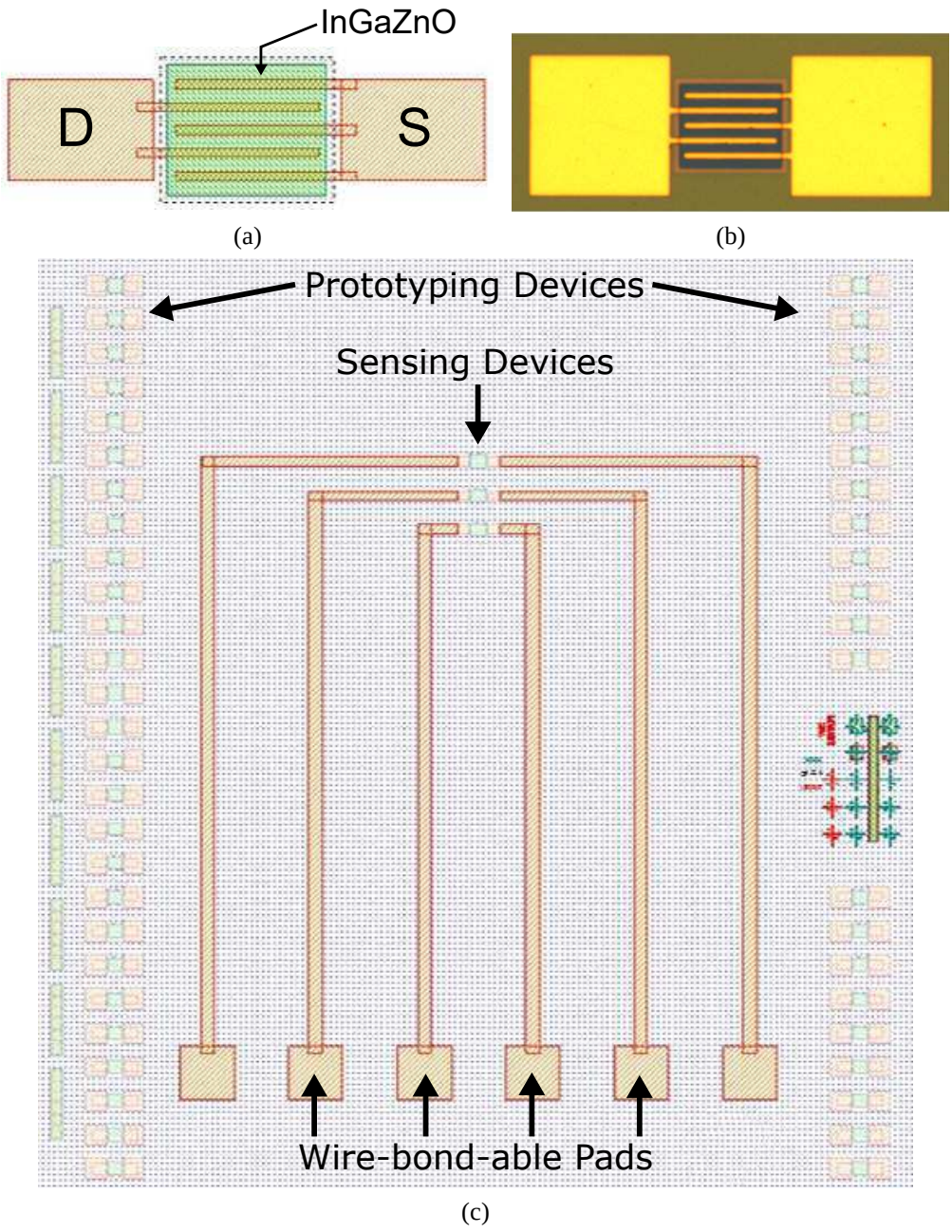


Figure 3.2. Generation 1 of InGaZnO TFTs: (a) device layout, (a) device picture, and (c) die-level layout.

since a gate metal layer does not need to be deposited and patterned, and (2) high quality, thermally grown SiO_2 can be used as the gate insulator. Hence, the first generation layout of TFTs (shown in Figure 3.2) used this this approach.

These devices used an inter-digitated finger topology for the S/D metal. This allows the formation of multiple parallel channels that increase the total drain current (Figures 3.2a

and 3.2b). On the die level, the TFTs were densely distributed along two columns on either side for rapid characterization. Additional devices were included in the middle of the die that were addressable via large wire-bond able pads. It was thought that this would facilitate packaging and microfluidic testing. Unfortunately, there were several shortcomings to this approach. First of all, the use of SiO_2 increased the threshold voltage of the devices due to the material's low dielectric permittivity. These large voltages increased the likelihood of hydrolysis if the devices were exposed to an aqueous environment. Secondly, the thermal oxide growth step was executed at very high temperatures (>1000 °C), which rendered this process incompatible with lower cost substrates such as glass, or flexible substrates in the future. Thirdly, the use of a common gate made it impossible to individually address the TFTs, thus ruling out the ability for sensor arrays. Lastly, it was discovered that the center devices were too close to each other, and therefore it was not possible to make separate microfluidic channels for these devices.

3.2.2 Generation 2

Given the shortcomings of the first generation design, a second generation layout was created (Figure 3.3). 5×5 mm^2 dies were designed with the intention of facilitating microfluidic packaging (Figure 3.3a). As such, space was alloted for three 300 μm wide microfluidic channels, each with 1 mm diameter inlet and outlet. The location of these channels defined three rows of devices, each with three TFTs. The probe pads were gathered on the edges of the die, and the metal routing was designed in order to minimize overlap with the microfluidic channels, in turn reducing the risk of hydrolysis. Each TFT was designed with its own bottom metal gate, making it possible to create sensor arrays in the future. This feature also necessitated the introduction of a via etching step to gain access to the bottom metal layer. The multi-finger concept was carried over, and devices with three different channel lengths were realized (i.e., L = 2, 5, 10 μm). This resulted in W/L ratios of 3082 (Figure 3.3d), 466 (Figure 3.3c), and 106 (Figure 3.3b), respectively.

These devices were extensively used in this thesis, in particular for both gas- and initial

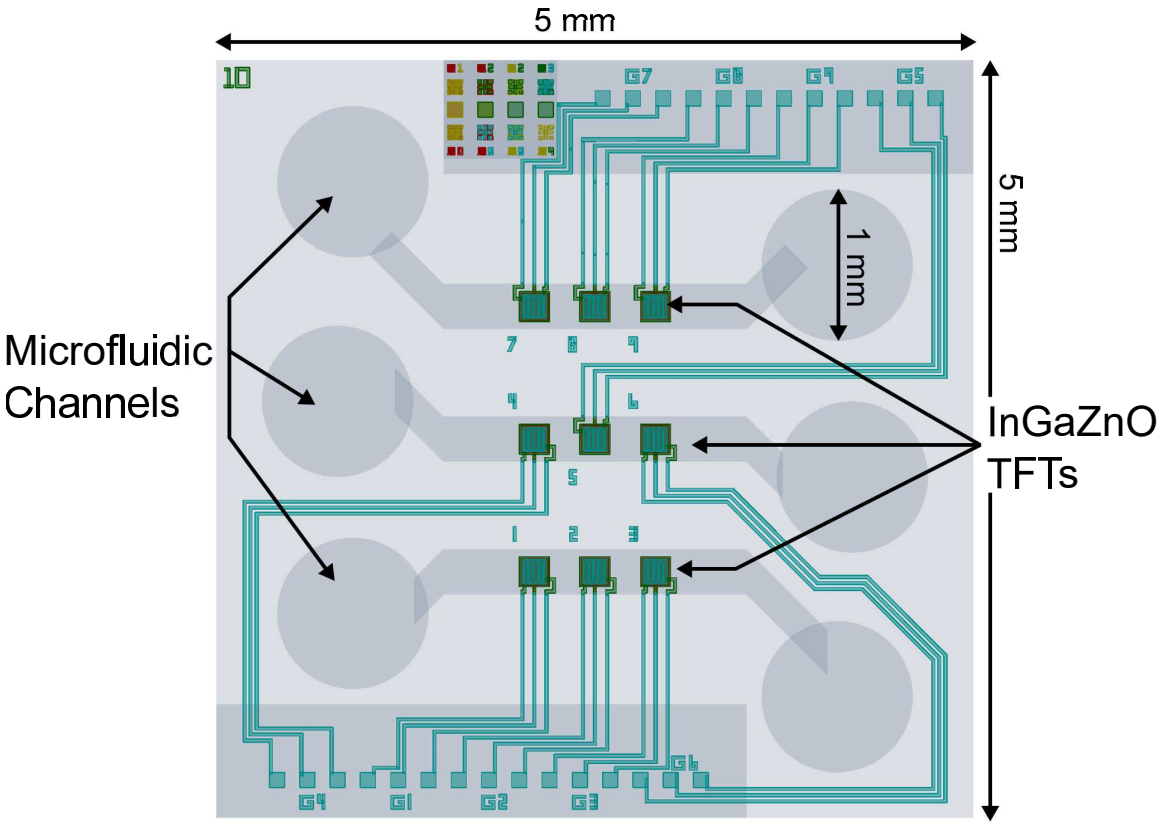


Figure 3.3. (a) Die-level layout with allocated space for microfluidic channel integration. Top-view photographs of Generation 2 InGaZnO TFTs: (b) L = 10 μm (W/L = 106), (c) L = 5 μm (W/L = 466), (d) L = 2 μm (W/L = 3082).

liquid-phase chemical sensing experiments. However, it was eventually realized that there remained a number of challenges with this design. Firstly, there were only three W/L ratios that could be evaluated, which did not permit the extraction of intrinsic performance

parameters using methods that require a wider range of geometries (to be discussed in Section 3.5.3). Moreover, the range of W/L ratios (106-3082) was very large in comparison to other works in the literature, making it difficult to benchmark the electrical performance of the TFTs (e.g., field-effect mobility) against the results presented by other groups. On a die-level, it was discovered that microfluidic package integration was still hindered by the small device-to-device separation and small inlet/outlet diameter (1 mm) that necessitated high alignment precision when connecting external tubing. Lastly, no material test structures (e.g., metal-insulator-metal capacitors) were included across the wafer, thereby ruling out the ability to carry out individual thin film material characterization.

3.2.3 Generation 3

The third and final iteration had three principle goals: (1) redesign the device-level layout in order to extract intrinsic device performance, (2) introduce test structures for thin film characterization and (3) develop a liquid-phase sensing die layout that would address the limitations of the second generation design and facilitate integration with PDMS microfluidic structures. The device and die layouts are discussed in this section, while the test structures are described in Section 3.4.

The first parameter that was considered in the device redesign was the sizing of the semiconductor layer. In both Generations 1 and 2, the outer border of the semiconductor layer lay outside of the S/D fingers. When considering a single channel (Figure 3.4a), this translates to a semiconductor layer width (W_{semi}) that is larger than the S/D contact width ($W_{S/D}$). The consequence of such a design is that the drain current can flow in the regions outside the S/D contacts, thus making the definition of the channel width and, consequently, the W/L ratio, ambiguous. This can be avoided by ensuring that $W_{semi} < W_{S/D}$, as shown in Figure 3.4b. In this case, the semiconductor width is clearly equivalent to the channel width.

The length of the semiconductor layer, specifically in terms of how much of an overlap exists between the S/D metal contacts and the semiconductor underneath, is also important.

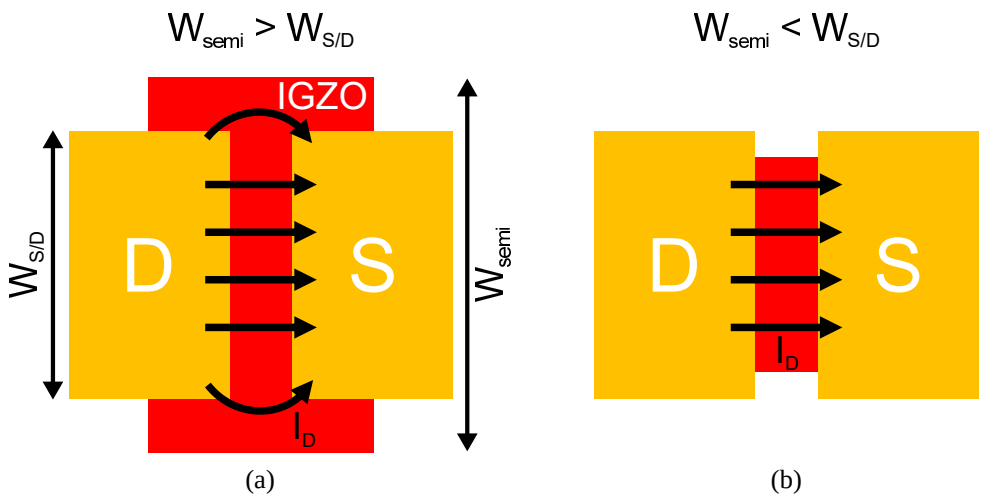


Figure 3.4. Comparison of current flow in a TFT when the width of the semiconductor (W_{Semi}) is (a) wider or (b) narrower than the width of the S/D metal contacts ($W_{S/D}$).

In Chapter 2, it was assumed that the electron exchange between the semiconductor channel and the source/drain contacts was uninhibited; in other words, that there was no contact resistance ($R_c = 0$). In practice, however, R_c cannot be altogether ignored. In Figure 3.5, the flow of current from the semiconductor layer into the metal source contact above is depicted. This current passes through a resistor network defined by the sheet resistance of the semiconductor (R_{sh}) and the contact resistance. The voltage drop across this network as a function of position ($V(x)$) is described by [124]:

$$V(x) = \frac{I_D \sqrt{R_{sh}\rho_c}}{W} \frac{cosh\left(\frac{L_c - x}{L_T}\right)}{sinh\left(\frac{L_c}{L_T}\right)} \tag{3.1}$$

where W is the contact width, L_c is the length of the contact (or the overlap between the semiconductor and the metal), ρ_c is the specific contact resistivity that determines R_c, and L_T is the transfer length. L_T represents the portion of the contact through which the majority of the drain current will flow and is defined as the length over which $1/e$ of the voltage is dropped:

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{3.2}$$

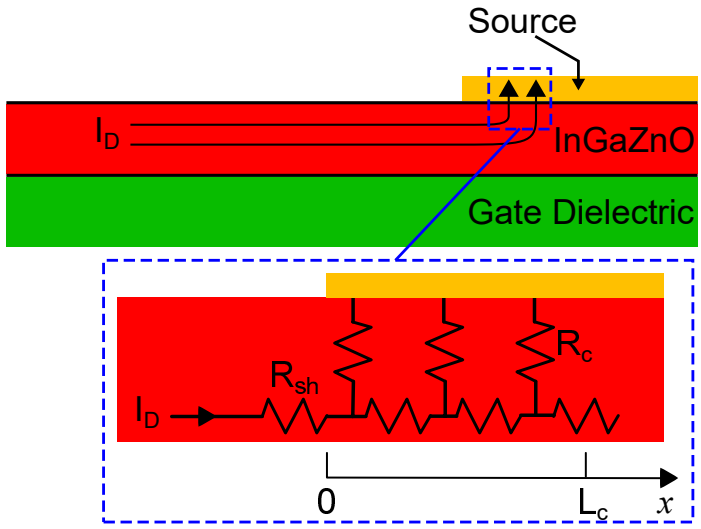


Figure 3.5. Cross-sectional view of the current flow from the semiconductor layer into source drain contact. The flow of current is affected by the sheet resistance (R_{sh}) of the semiconductor, as well as the contact resistance (R_c) between the semiconductor and the metal contact. Adapted from [124].

Thus, if $L_c >> L_T$, then $R_c = \rho_c/L_T W$, but if $L_c \sim L_T$, then $R_c = \rho_c/LW$. More details about how to experimentally extract L_T and R_C will be presented in Section 3.5.3. In terms of their impact on the device layout, it is desirable in TFTs that $L_c > L_T$. Since other works have shown that the transfer length is usually ~1 μm [148, 149], and in order to facilitate reliable alignment, L_c was set to 10 μm.

A further consideration in the redesign was the overlap between the gate metal and the S/D metal layers. In the previous generations, the gate contact was made very large and therefore completely overlapped with the S/D contacts. However, this overlap introduces a parasitic capacitance (C_{GS}) that directly influences the high-frequency performance of a TFT [150]:

$$f_T = \frac{g_m}{2\pi C_{GS}} \propto \frac{\mu}{L\,(L + L_{ov})} \tag{3.3}$$

where f_T is the transit frequency at which the gain of a field-effect transistor is unity, g_m is the transconductance and L_{ov} is the overlap between the gate metal and the source or drain metal. As a result, the gate contact was narrowed and L_{ov} was made 5 μm.

With the above constraints in mind, TFTs were designed with a channel width of 100

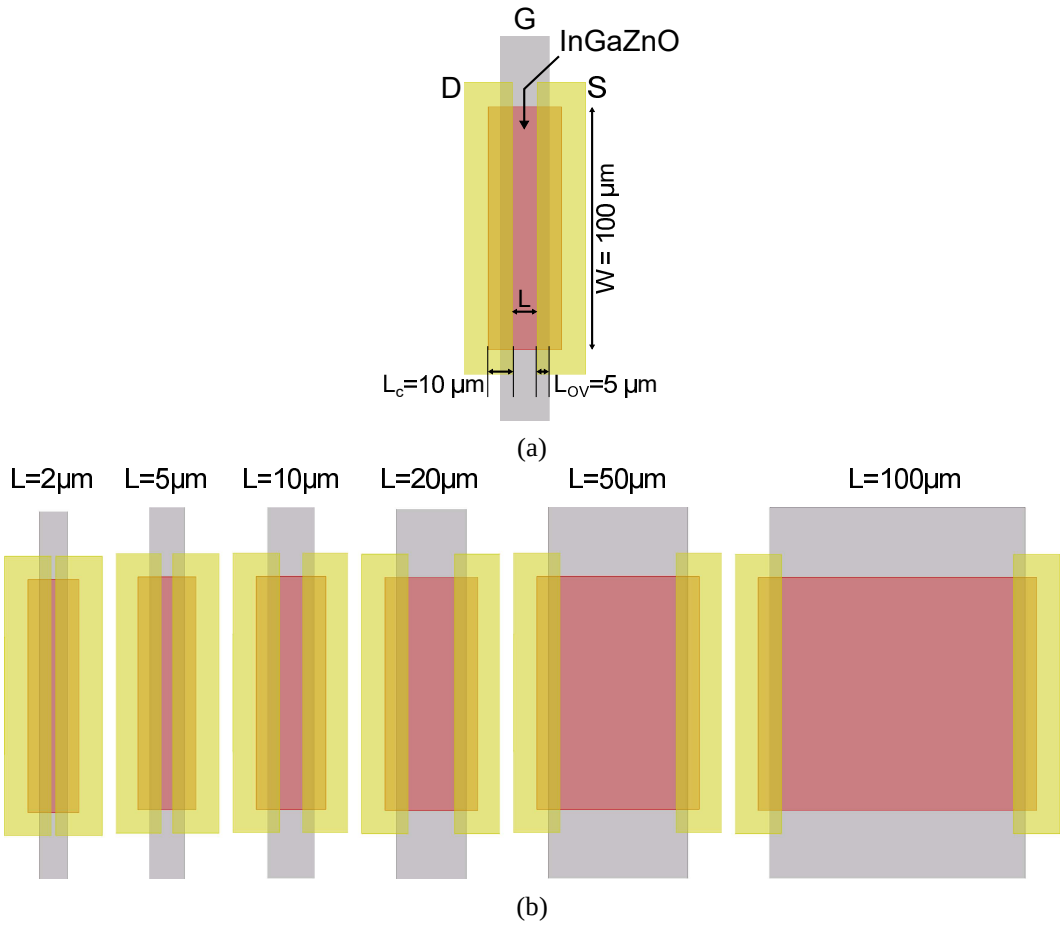


Figure 3.6. Generation 3 TFT Layouts: (a) individual TFT with W = 100 µm and L = 10 µm, and (b) overview of all TFTs with varying lengths ranging from 2 µm to 100 µm.

µm and a range of lengths, L = 2, 5, 10, 20, 50 and 100 µm. This corresponds to W/L ratios of 50, 20, 10, 5, 2, and 1, respectively. The layout of these devices is shown in Figure 3.6.

To extend the lifetime of these devices in liquid, the sensing dies were also redesigned (see Figure 3.7). Compared to the second generation, the die dimensions were increased from 5 mm × 5 mm to 12.5 mm × 15 mm. This adjustment permitted larger inlet and outlets to be used in order to facilitate the attachment of external tubing. Secondly, the number of TFTs per die was reduced from nine to six, thereby requiring less metal wiring and consequently allowing the metal traces to be spaced out further in order to reduce electric field strength and reduce the risk of hydrolysis/faradaic leakage currents. Thirdly, two new masks, which are discussed in more detail in Section 6.4.1, were created for SU-8 and PDMS. The SU-8 mask exposes the InGaZnO TFT pH sensing area as well as the outer

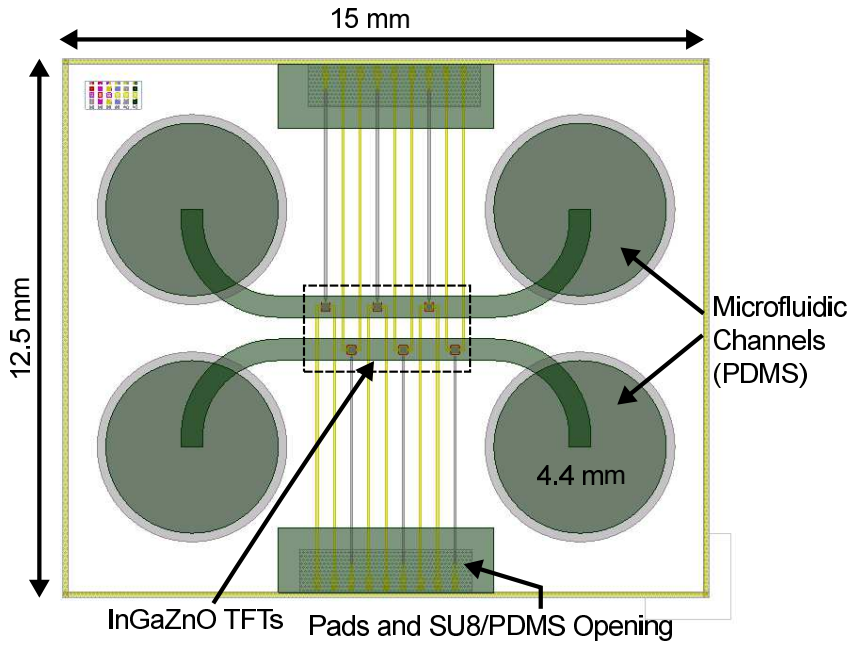


Figure 3.7. Third generation sensing die layout for microfluidic packaging.

contact pads. The PDMS mask is used to create a Si-wafer based mold for PDMS casting. This PDMS is then used as a capping layer of the SU-8 defined microfluidic channels.

3.3 InGaZnO Thin Film Transistor Fabrication

The wafer-scale microfabrication process that was developed to manufacture InGaZnO TFTs is presented in this section. Examples of two fabricated TFTs using the third generation layout are shown in Figure 3.8. The light yellow traces are the top (S/D) metal, while the darker metal is the bottom (G) metal. A via has been created in order to connect to the bottom metal through the gate dielectric layer, which otherwise covers the entire wafer. The boundaries of the InGaZnO layer can also be observed. In the following text, an overview of the fabrication processes is first provided, followed by more detailed descriptions of the key thin film deposition methods.

3.3.1 Fabrication Process Overview

The standard fabrication process employed in this work (Figure 3.9) involves the use of a Si wafer substrate. Due to the low temperature budget of the overall process, however,

it is possible to substitute Si with alternative materials, such as glass and certain plastics. This was demonstrated via successful fabrication of TFTs on glass within the Georgia Tech IEN cleanroom (Section 3.5.1.1). Glass-based TFTs are also investigated in Chapter 7 as phototransistors, and these devices were fabricated at the National Chiao Tung University (NCTU) cleanroom facilities in Taiwan. Details regarding their specific fabrication flow are included in that chapter. Nonetheless, in the event that Si is used, a non-conducting isolation layer must first be grown in the form of a 1 μm thermal SiO_2 layer.

Thereafter, formation of the bottom metal gate contact (M1 layer) must be undertaken. The strategy for this depends on the material that is used. In the Generation 2 TFTs, aluminum (Al) was adopted because it can be reliably dry etched to achieve the small features (i.e., down to ~2μm) used in capacitive sensors that were concurrently fabricated with the same mask set. 200 nm of aluminum was first electron beam (e-beam) evaporated onto the SiO_2, followed by a lithography step for patterning. Over the course of multiple wafer runs, it was observed that subsequent deposition steps, such as the InGaZnO deposition, would occasionally roughen the Al, creating so-called hillocks that pierce through the gate dielectric and prevent the TFT from functioning. This motivated the transition to 25/200 nm thick chrome/gold (Cr/Au) gate metalization for the Generation 3 devices. Since Au is

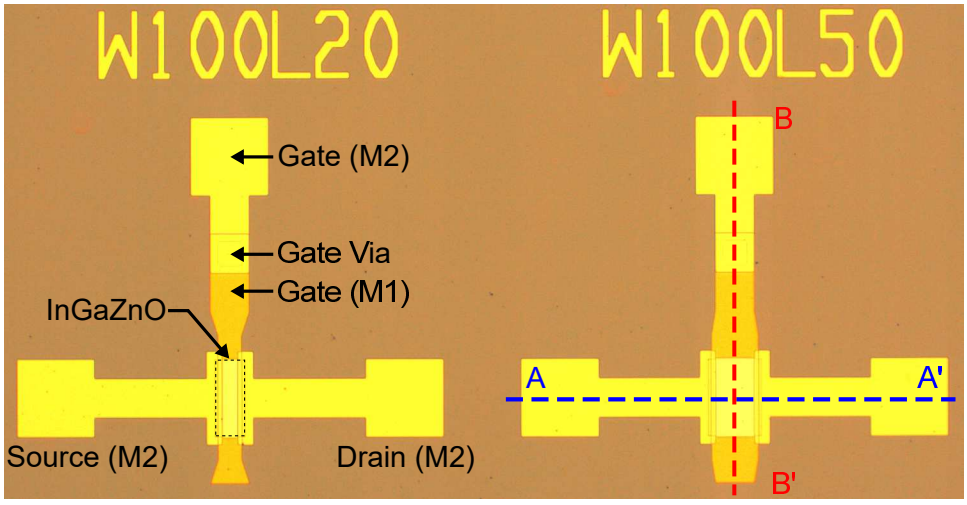


Figure 3.8. Top-view photographs of fabricated L=20 μm and L=50 μm InGaZnO TFTs.

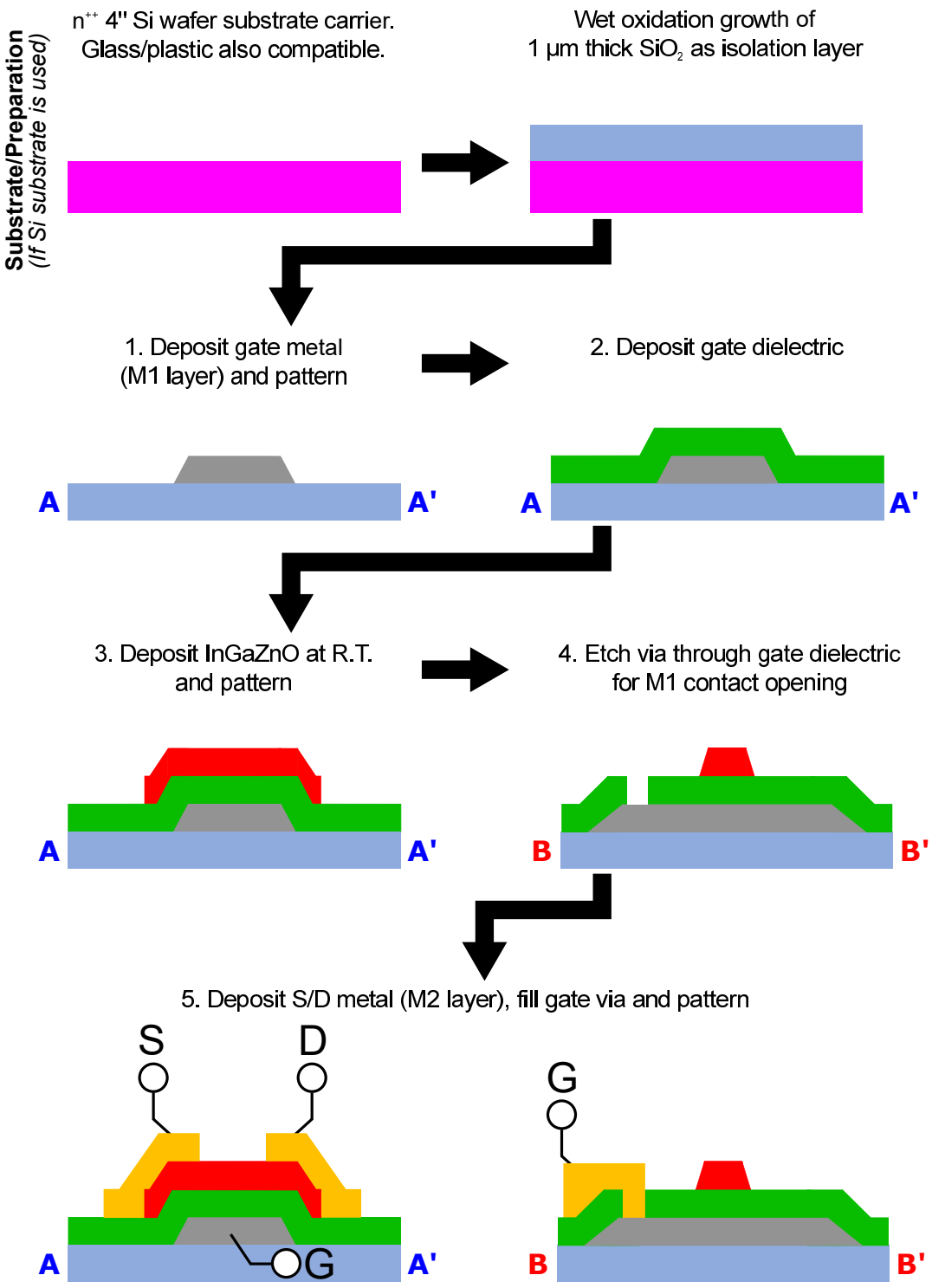


Figure 3.9. Overview of low-temperature InGaZnO TFT fabrication process.

notoriously difficult to etch, lift-off was instead employed to create the gate contact.

The gate dielectric is then deposited. In Generations 1 and 2, traditional dielectric deposition techniques were used, such as plasma-enhanced chemical vapor deposition (PECVD). This had two drawbacks: (1) the available materials have relatively low dielectric constants (e.g., ϵ_r of SiO_2 is ~3.9), and (2) the deposition temperature is usually ~300 °C, which incompatible with many flexible substrates. To address both of these issues, alumina (Al_2O_3), with ϵ_r of ~9, was deposited using atomic layer deposition (ALD) instead. The temperature for this step was 180 °C, with the flexibility to be reduced below 100 °C, if necessary. Moreover, high-quality and very thin films of 50 nm thickness could be reliably obtained using this method. More details on the ALD deposition is provided in Section 3.3.3.

A 50 nm InGaZnO semiconducting film is then deposited on top of the gate dielectric. In this work, this is accomplished via either RF sputtering at the Georgia Tech IEN or pulsed laser deposition (PLD) at the Sensors Directorate of the Air Force Research Laboratory (AFRL). The film is patterned using a mesa etch step involving diluted glacial acetic acid in DI water (1:150). More details regarding these two deposition processes and the corresponding parameters are presented in Section 3.3.2.

In order to connect to the bottom M1 metal layer used for the gate contact, a via must be created through the gate dielectric. For this step, dry etching is used to locally remove the Al_2O_3. In the last step, the S/D contacts must be formed and the gate via needs to be metalized. Rather than first depositing the second metal (M2 layer), and subsequently etching it, lift-off is used. The motivation behind this decision is that both chemical wet etching and plasma dry etching can harm the exposed InGaZnO layer [151]. One way to prevent this is to employ an etch-stop process flow [139, 152]. For simplicity and to maintain flexibility in the choice of passivation material (discussed in Chapter 5), this work uses lift-off in stead. This process involves gentle solvent removal of photoresist and any overlying metal simultaneously in unwanted regions. Thus, 25/200 nm thick Cr/Au S/D contacts were made to the InGaZnO.

3.3.2 InGaZnO Deposition

As InGaZnO technology has matured, a number of low-temperature deposition techniques have been developed for this semiconductor material. These include pulsed laser deposition (PLD) [130], radio-frequency (RF) sputtering [153], direct-current (DC) sputtering [154], and even solution processing [155] that can be leveraged for ink-jet printed electronics. As mentioned above, the two deposition methods employed in this work are RF sputtering and PLD. In the following section, these two techniques are described in more detail.

3.3.2.1 Radio-Frequency Sputtering

Sputtering is a type of physical vapor deposition in which a target (e.g., InGaZnO) is bombarded with heavy ions in order to eject atoms from the target's top surface and transfer them to a substrate (e.g., Si wafer). The sputtering ions are usually obtained through plasma ionization of an inert gas, such as argon (Ar), and are consequently accelerated towards the target by placing it on the cathode. DC sputtering is used extensively for the deposition of metals, particularly in cases where excellent step coverage is required. However, a DC bias cannot be used to deposit dielectrics due to the building up of charge on the dielectric target's surface, which causes charge screening and hampers deposition. This can be avoided through the use of an alternating current (AC), or radio-frequency (RF), plasma bias.

There are several process parameters that can be controlled, including RF power, pre-deposition pressure, deposition pressure and substrate temperature. Initial depositions of InGaZnO at Georgia Tech were done using the Kurt J. Lesker PVD75 RF sputtering tool. This tool presented challenges, such as target overheating (and damage, in some cases), relatively high pre-deposition pressure (i.e., $\sim 2 \times 10^{-5}$ Torr), and the lack of a shutter to prevent deposition during the long plasma ramp-up and ramp-down periods that were necessary to minimize thermal shock to the target material. This led to the eventual use of the Denton Discovery RF/DC Sputtering system that possesses a target shutter, a load-lock chamber that alleviated the need to vent the deposition chamber when loading and unloading samples. This translated in a reduced pre-deposition pressure consistently in the range

of $\leq 2 \times 10^{-6}$ Torr, which is preferred in order to ensure the purity of the deposited thin films. In general, applying heat to the substrate holder improves the quality of the deposition. However, semiconducting InGaZnO can be reliably obtained at room temperature, which provides the added benefit of compatibility with low-cost glass and plastic substrates that have lower melting or glass transition temperatures compared to Si. Intuitively, the RF power plays a major role in determining the deposition rate. For InGaZnO, it has also been found to greatly affect the resistivity of the deposited thin films [144]. To gain further control over the InGaZnO properties obtained with this method, reactive oxygen species can also be introduced into the chamber. By tuning the partial pressure of oxygen, the number of oxygen vacancies, and hence the doping density and the mobility can all be adjusted [135, 153] (recall the discussion in Section 2.3.1). Oxygen has also been found to affect InGaZnO TFT stability [156].

3.3.2.2 Pulsed Laser Deposition

This deposition technique is another example of physical vapor deposition, wherein a pulsed laser beam is directed towards a target in order to ablate it and bring about deposition onto a nearby substrate. Though sputtering has seen a more successful industrial acceptance compared to PLD due to its scalable nature, the latter still remains a powerful and valuable research tool. In a similar fashion to sputtering, the laser energy, the pulse frequency, the deposition pressure, the oxygen partial pressure, and the substrate temperature can all be adjusted to control the deposition of InGaZnO. The uniformity of the deposition is improved by rotating the substrate, as well as scanning the laser beam across the target.

The Sensors Directorate at AFRL possesses a dedicated ZnO/InGaZnO PLD system, which minimizes the effects of material cross-contamination. State-of-the-art polycrystalline ZnO TFTs have been produced by this system with high frequency operation reaching the GHz regime [39, 136, 157].

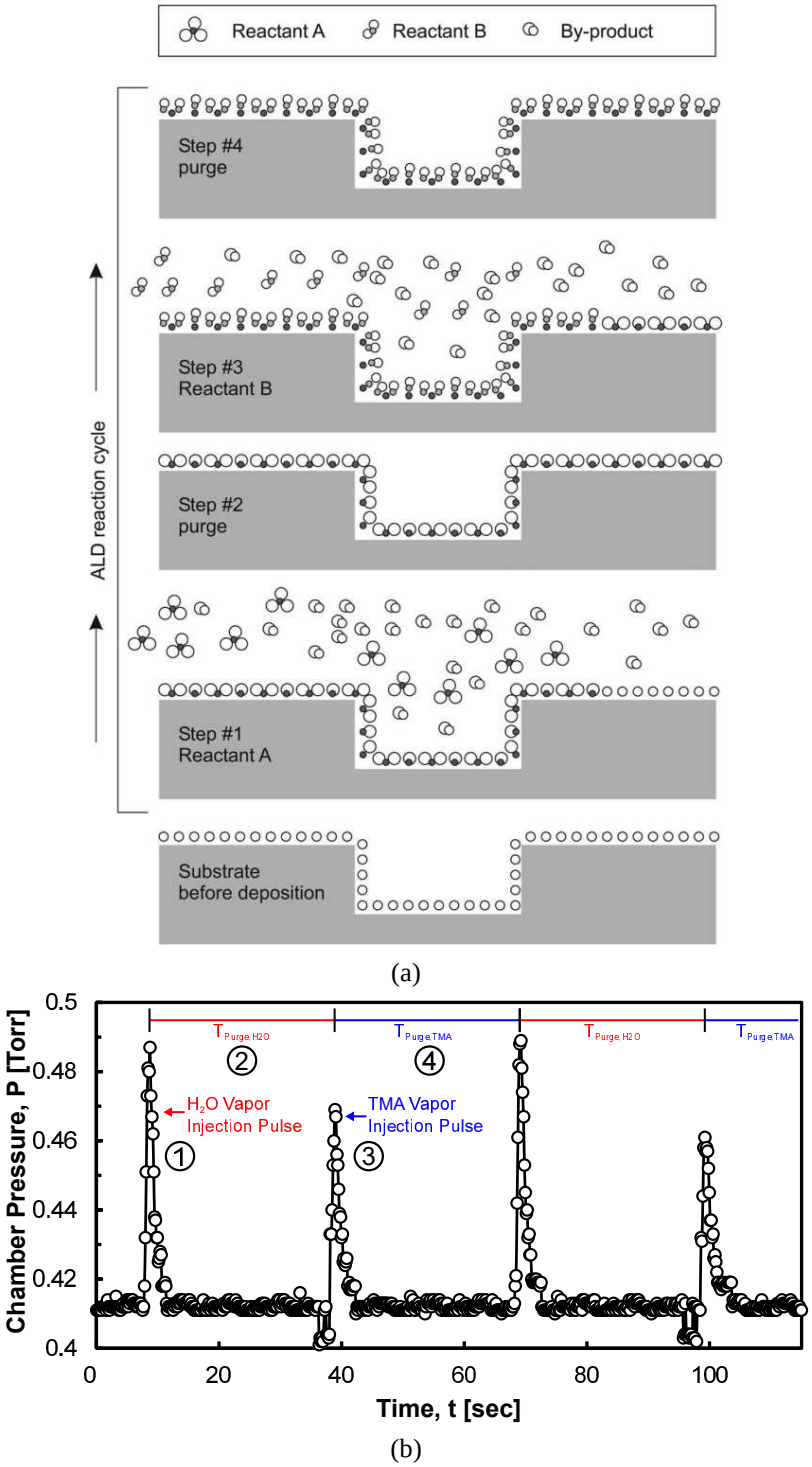


Figure 3.10. Atomic layer deposition: (a) generalized schematic overview of process sequence [158], and (b) temporal chamber pressure profile during ALD of Al_2O_3 using the Cambridge Nanotech ALD system at Georgia Tech IEN.

3.3.3 Atomic Layer Deposition for High-ϵ_r Dielectric Deposition

As described in Section 3.1 above, the choice of gate dielectric material plays a major role in determining the threshold voltage, as well as the influence of gate leakage. In this thesis, atomic layer deposition (ALD) is used to deposit the gate dielectric, since it allows for the high-quality and conformal growth of dielectric films at low temperature with sub-nm thickness control [158, 159]. This unique control over thickness is made possible by exploiting self-saturating chemical reactions between two precursor gases. Figure 3.10a describes how ALD can be broken down into four fundamental steps that are be repeated during each cycle of deposition. In Step 1, a reactive precursor gas (Reactant A) is introduced into a deposition chamber and distributes across the surface of the sample. Inert Ar is then flushed through the chamber in Step 2 in order to purge any traces of Reactant A that have not adsorbed to the sample's surface. Step 3 sees the introduction of a second precursor gas (Reactant B) that reacts with Reactant A molecules. This reaction forms a film on the substrate surface. Any by-products of the reaction between Reactant A and B are then removed from chamber in Step 4. It is crucial that the chemical reactions in Steps 1 and 4 are self-terminating, meaning that reactants only react with their complements. In other words, once reactant B reacts with any available reactant A molecules, it cannot react with other reactant B molecules to continue film deposition. Further deposition or growth will only occur once more reactant A molecules are added.

Figure 3.10b provides an example of a typical chamber pressure profile during ALD, specifically for the case of Al_2O_3, which has been used in this thesis. Step 1 is identified by a pressure spike that corresponds to the rapid injection of the first reactant, which is water vapor. This is followed by a delay during which the pressure recovers and left-over water vapor is removed from the chamber. In Step 3, an additional pressure spike is observed, this time representing the pulse injection of the metalo-organic precursor, TMA (trimethylaluminum). TMA reacts with the water vapor on the sample surface to produce a single molecular layer of Al_2O_3. A purge is carried out once again, following by the

beginning of a new deposition cycle that is signaled by another water vapor pressure spike.

In ALD, the deposition rate (e.g., Å/min) depends on the ratio of two components: time/cycle and thickness/cycle. Since the purge steps are driven by diffusion, the duration of these steps depends highly on the temperature at which the deposition is done. Namely, the lower the deposition temperature, the longer each purge step must be made in order to ensure that left-over by-products are evacuated from the chamber. The thickness per cycle depends on multiple factors [158], but for Al_2O_3 studied in this work, it has generally been observed to decrease as the temperature rises.

3.4 Thin Film Characterization

Characterization of thin films following deposition is critical to controlling the fabrication processes described above, as well as reliably extracting the performance characteristics of the resulting TFTs. For example, calculation of the field effect mobility (see Equations 2.23 and 2.21) require prior knowledge of the dielectric layer's capacitance (per area). This, as well as other interesting characteristics, can be measured through the use of metal-insulator-metal (MIM) and meta-insulator-semiconductor (MIS) structures shown in Figure 3.11. A "Greek Cross" design was adopted as it allows for precise definition of the capacitor's area, and is immune to x- and y-axis misalignment. Five capacitor sizes were laid out in order to rule out the presence of unexpected scaling effects.

3.4.1 Metal-Insulator-Metal (MIM) Capacitors

The MIM capacitor is a 3-layer device that is fabricated during the same fabrication run as the TFTs. It consists of a gate dielectric layer sandwiched between the top and bottom metal layers. The capacitors in this study consist of an Cr/Au - Al_2O_3 - Cr/Au stack. The Al_2O_3 layer is 50 nm thick, and was deposited at 180 °C via ALD. Figure 3.12 shows the dependence of the capacitance (green) and the capacitance density (red) on the area. These measurements were obtained on-wafer in the absence of a DC bias, at 10 kHz and a 50 mV AC voltage using an Agilent 4284a LCR Meter. As expected, given Equation 2.1, the

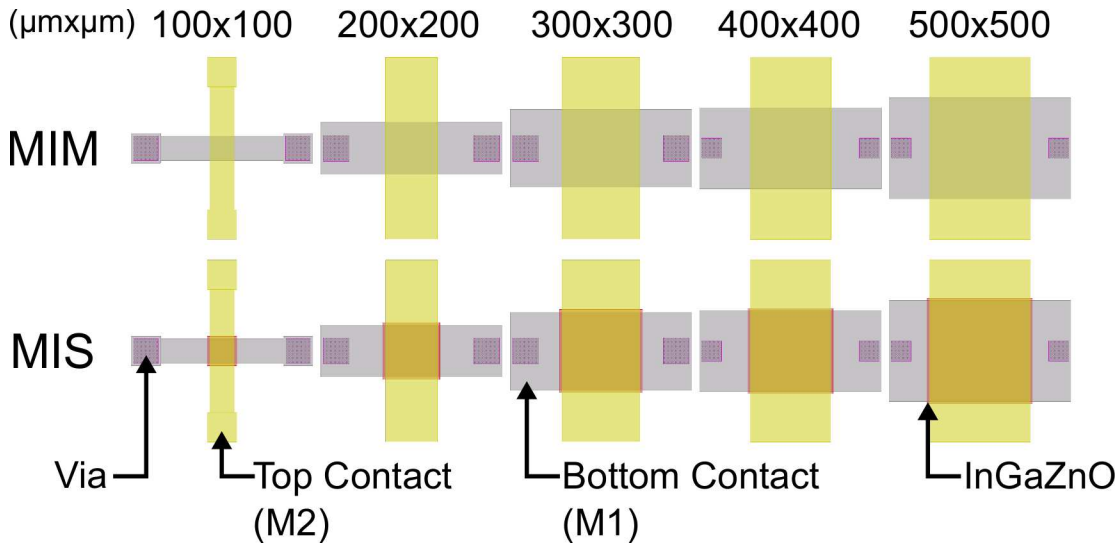


Figure 3.11. Overview of the MIM and MIS capacitor layouts for thin film characterization.

capacitance increases linearly as the area is increased, from 14.1 pF for the $100 \times 100 \mu m^2$ capacitor to 344 pF for the $500 \times 500 \mu m^2$ capacitor. The capacitance density is found by dividing the capacitance by the area, and was calculated to vary between 137.9 and 141.7 nF cm^{-2} across the range of areas investigated. All in all, this information can then be used to conclude that ϵ_r=8. This is slightly lower, yet still comparable to the value of ϵ_r=9 found in [142].

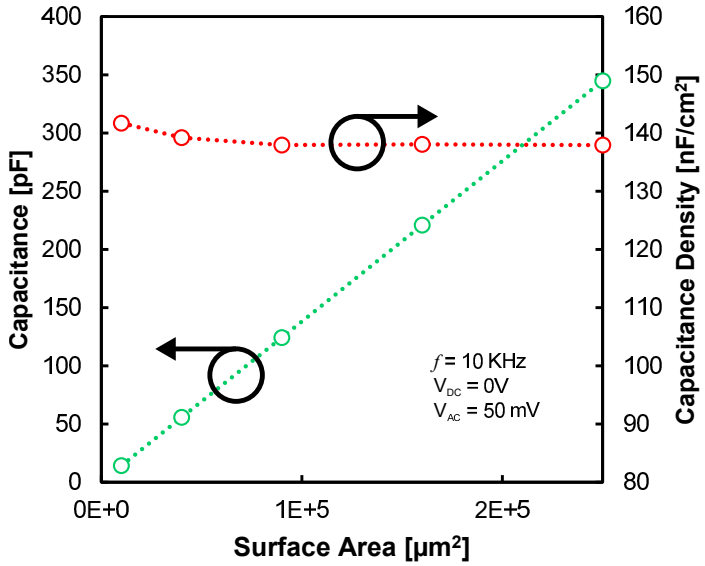
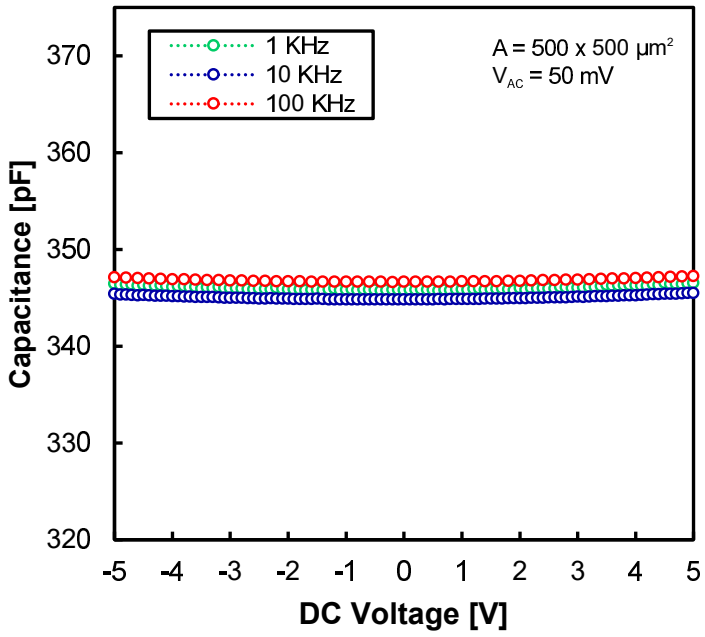


Figure 3.12. Capacitance and capacitance density versus capacitor area, using a 50 nm thick Al_2O_3 deposited by ALD.

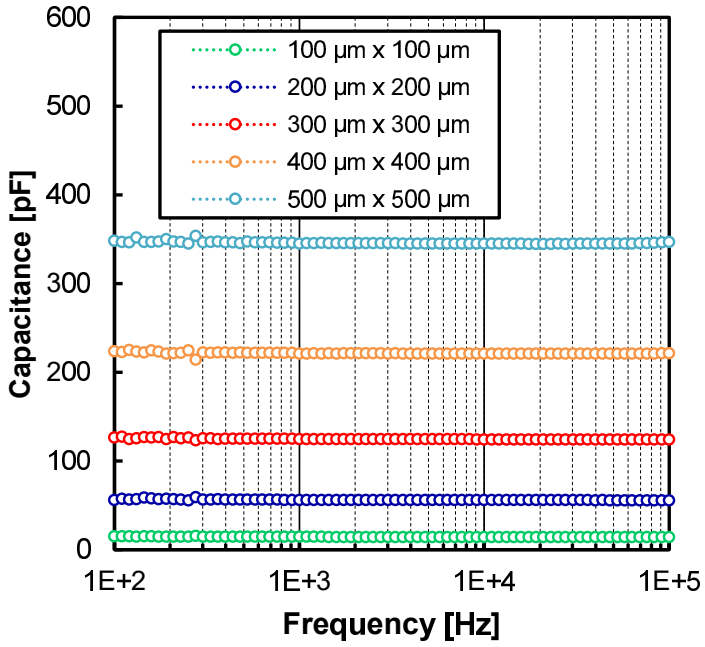
To further assess the quality of the dielectric, it is also important to examine how the capacitance varies with DC voltage and with frequency. DC voltage sweeps between -5 and +5 V were conducted on the $500 \times 500 \mu m^2$ capacitor at 1, 10 and 100 kHz (see Figure 3.13a). It was observed that the value of capacitance varied no more than 0.9% at each frequency over the entire voltage range, and less than 1.2% over the entire dataset. In Figure 3.13 capacitor vs. frequency characteristics are displayed for all of the capacitors without a DC bias. It is evident that frequency stability is also achieved. These results indicate the high quality ALD of Al_2O_3.

3.4.2 Metal-Insulator-Metal (MIS) Capacitors

In Section 2.1.2, it was shown that the core structure within any TFT is the three-layer MIS capacitor. For practical testing, however, the capacitor is actually a four-layer structure, consisting of (bottom to top) Cr/Au - Al_2O_3 - InGaZnO - Cr/Au. The Al_2O_3 is the same as the one analyzed in the previous section. The InGaZnO is obtained via RF sputtering. C-V measurements were collected using a $500 \times 500 \mu m^2$ MIS capacitor at 1, 10 and 100 kHz with a AC voltage of 50 mV. The DC voltage was swept from -5 to +10 V. For all three frequencies, it was found that at low voltages, when the InGaZnO is depleted, the capacitance was 315-320 pF, which corresponds to the series addition of the dielectric and depletion region capacitances. As the voltage is increased, a transition region is observed in which the capacitance increases before reaching a semi-saturated state. The value of the capacitance in the saturated region, where accumulation occurs, was 335-340 pF, which roughly corresponds to the capacitance observed in the MIM structure of same dimensions. Thus, when the device is OFF the series capacitance of $C_{InGaZnO,depl}$ and C_i are observed. After the onset of accumulation, however, the total capacitance increases and is dominated by C_i alone. It should be noted that the frequency dependent threshold voltage is indicative of the presence of interface charge traps [121, 160, 161], whose importance in the context of bias stress stability will be discussed in Section 4.3.



(a)



(b)

Figure 3.13. Behavior of MIM capacitor using 50 nm ALD Al_2O_3 dielectric: (a) capacitance-voltage characteristic for a $500 \times 500\ \mu m^2$ capacitor, (b) capacitance-frequency response for all capacitor sizes.

3.5 TFT Characterization

In this section, the characterization of fully fabricated InGaZnO TFTs is discussed. Comparisons are made between devices utilizing InGaZnO RF sputtered at Georgia Tech or PLD deposited at AFRL, as well as between on-glass and on-Si TFTs with RF sputtered

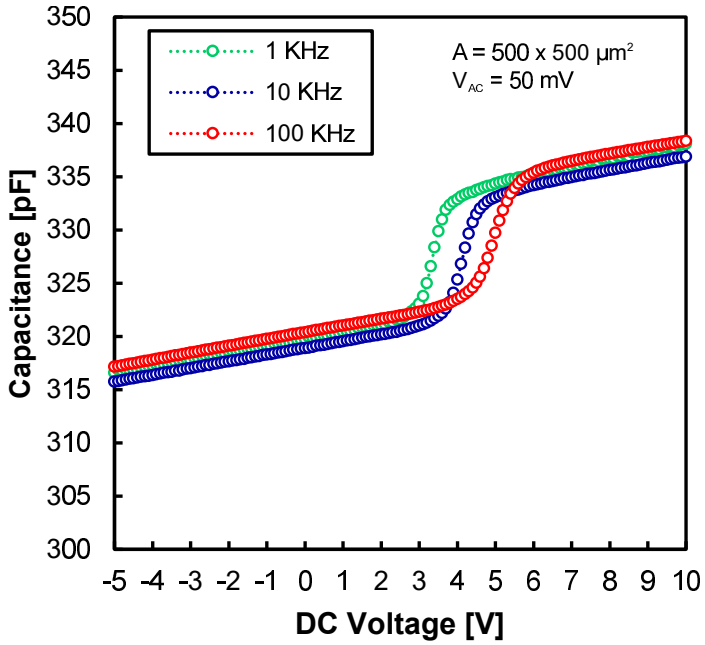


Figure 3.14. Capacitance vs. voltage behavior of an MIS capacitor comprising of a 50 nm **ALD Al_2O_3 dielectric and a 50** nm **RF-sputtered InGaZnO semiconductor.**

InGaZnO.

3.5.1 RF Sputtered InGaZnO TFTs

The effects of adjusting the major sputtering conditions (i.e., RF power, pressure and oxygen content) have been reported by previous groups [85, 137, 144]. Moreover, it has been found that post-process annealing can be used to improve performance over as-deposited films [162–164]. In this work, annealing is performed in air on a hot plate at 300 °C. In Figure 3.15 and Table 3.1, the effects of the O_2 annealing step on RF sputtered InGaZnO TFTs is shown, where RF sputtering was done with 150 W RF power (P_{RF}), 3 mTorr deposition pressure (P_{dep}) and 1% O_2 content within an Ar atmosphere. These devices have a

Table 3.1. Effect of O_2 annealing on RF sputtered InGaZnO (150 W**, 3 mTorr, 1% O_2) TFTs with W/L ratio of 106 (see Figure 3.15).**

State	$V_{TH,pos}$ [V]	$V_{TH,neg}$ [V]	S [mV/dec]	$I_{ON/OFF}$	$\mu_{FE,SAT}$ [$cm^2\ V^{-1}\ s^{-1}$]
Original	3.6	4	348	10^{10}	14.8
Post Annealing	4	4.7	270	10^{10}	5.3

50 nm thick ALD Al_2O_3 dielectric, and were made using the second generation layout. It is observed that annealing shifts the threshold voltage upwards. This indicates that, during annealing, oxygen vacancies that are present within the InGaZnO become occupied, in turn acting as charge acceptors and increasing sheet resistance. In line with the mobility-carrier density relationship in Figure 2.8, the reduction of carriers also results in a decrease of the mobility. In addition to these phenomena, it is also observed that S reduces after annealing from 348 mV/dec to 270 mV/dec, indicating that traps and defects originally present in the device are partially passivated. Further benefits of post-process/fabrication annealing in terms of device uniformity and bias stress stability are presented in Section 4.3.

3.5.1.1 InGaZnO TFTs on Glass

The above RF sputtered devices were fabricated on Si wafers for ease of handling. However, TFTs were also fabricated on glass substrates (Figure 3.16a) to demonstrate the viability of transferring the fabrication process to alternative substrates. The InGaZnO RF sputtering and ALD Al_2O_3 deposition conditions were maintained the same as before for

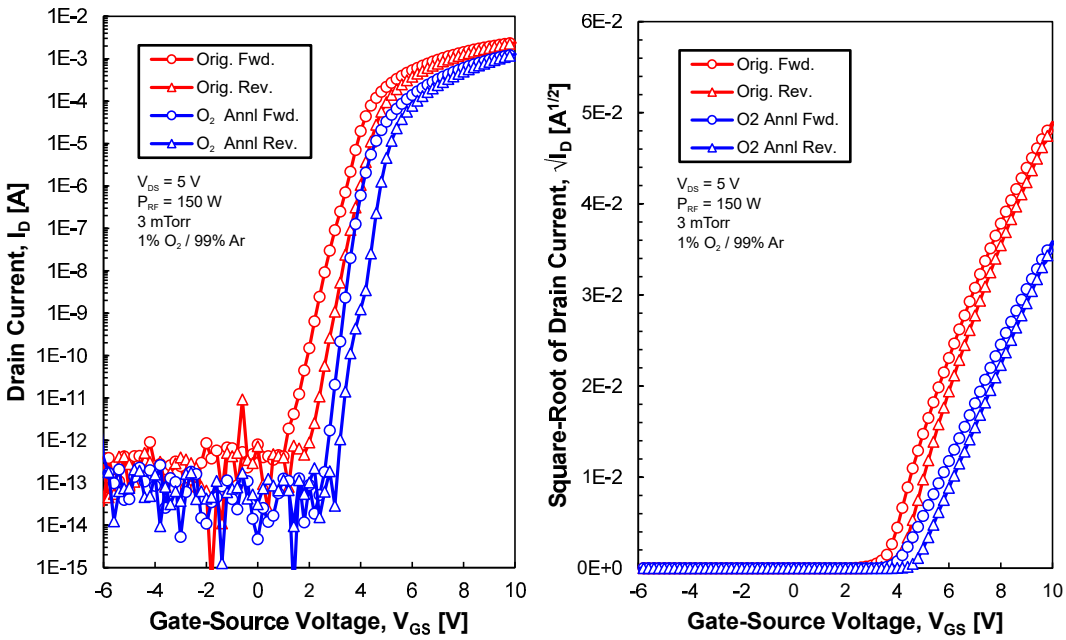
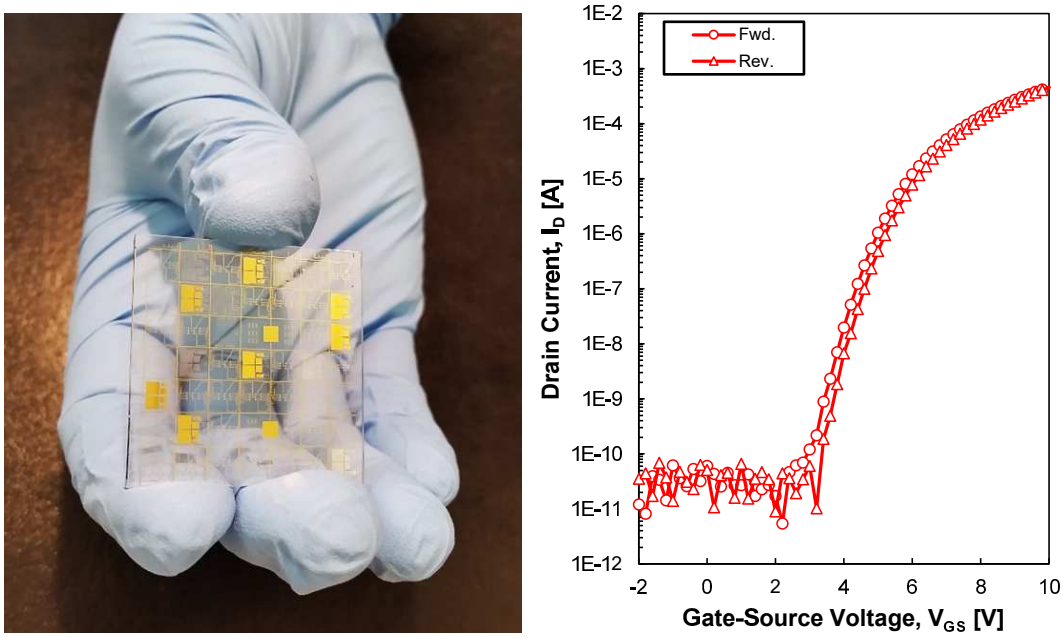


Figure 3.15. Transfer characteristics (V_{DS}) for RF sputtered InGaZnO TFTs with W/L ratio of 106: effect of post-fabrication O_2 annealing on (a) $\log_{10}(I_D) - V_{GS}$ and (b) $\sqrt{I_D} - V_{GS}$.



(a) (b)

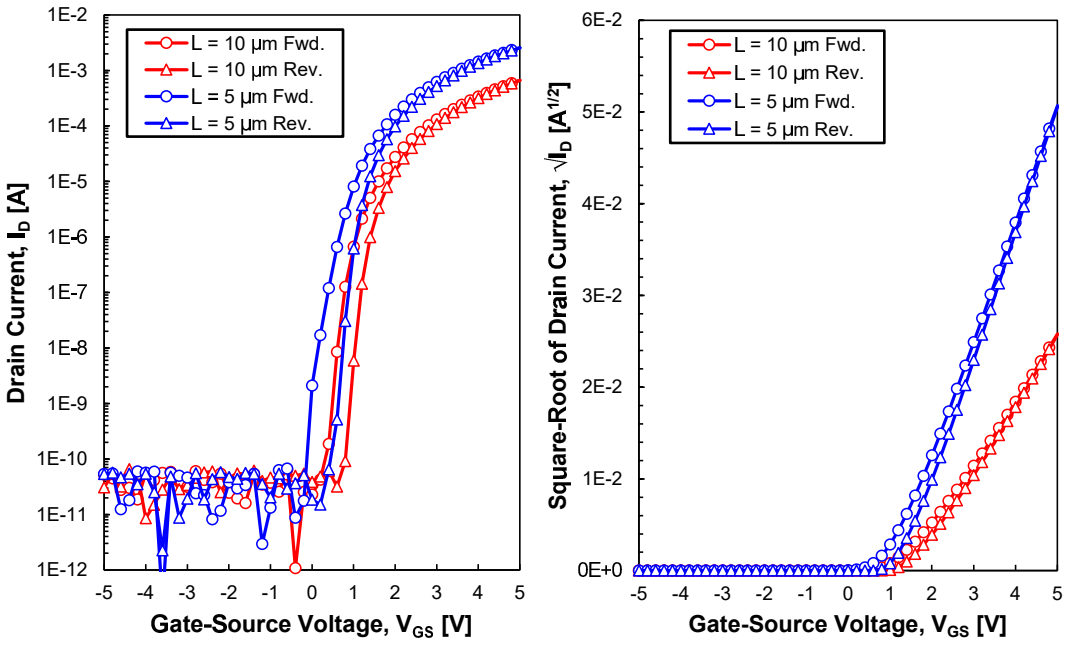
Figure 3.16. (a) Top-view photograph of InGaZnO TFTs fabricated on glass substrate and (b) transfer characteristic (V_{DS} = 5 V) for a W=1060/L=10 μm device in this batch.

fair comparison. I-V characteristics for these devices revealed V_{TH} = 5.1 V, $\mu_{FE,SAT}$ = 3.3 $cm^2\ V^{-1}\ s^{-1}$, S = 420 mV/dec and on/off ratio of 10^7. Though the performance has degraded slightly compared to the TFTs realized on Si, the performance is still sufficient for sensor deployment.

3.5.2 PLD InGaZnO TFTs

Figure 3.17 provides I-V characteristics collected from Generation 2 TFTs fabricated using PLD InGaZnO (1:1:1) from the Air Force Research Lab (AFRL), and annealed in an oxygen environment for 30 min at 300 °C. The transfer characteristic (V_{GS} vs. I_D) has been plotted on a logarithmic scale for two devices, one with L = 5 μm and the other with L = 10 μm, in Figure 3.17a. It can be clearly seen that the L=5 μm device conducts more current, due to the higher W/L ratio for this device (466 vs. 106). A summary of extracted characteristics is presented in Table 3.2.

Devices using the Generation 3 layout were also fabricated using PLD InGaZnO of two different compositions, 1:1:1 and 1:1:5. These were made using a conductive p++



(a) (b)

Figure 3.17. Comparison of (a) $I_D - V_{GS}$ and (b) $\sqrt{I_D} - V_{GS}$ between Generation 2 PLD-InGaZnO (1:1:1) TFTs with L = 10 µm and 5 µm (W/L=466) (V_{DS} = 5 V).

Table 3.2. Overview of Generation 2 PLD-InGaZnO (1:1:1:) TFT characteristics for two different W/L ratios (saturation mode, V_{DS} = 5 V).

Characteristic	L = 5 µm	L = 10 µm
Width [µm]	2330	1060
W:L Ratio	466	106
$V_{TH,pos}$ / $V_{TH,neg}$ / ΔV_{TH} [V]	1.04 / 1.30 / 0.26	1.25 / 1.49 / 0.24
On/Off Ratio	10^9	10^8
S_{pos} / S_{neg} [mV/dec]	184 / 185	241 / 233
$\mu_{SAT,pos}$ / $\mu_{SAT,neg}$ [cm^2 V^{-1} s^{-1}]	4.7 / 5.3	6.6 / 7.6

Si wafer common back gate and 25 nm thick ALD Al_2O_3 deposited at AFRL at 250 °C. Characterization of this Al_2O_3 film using the MIM capacitor structures described above found that ϵ_r=9. I-V characteristics for these devices are shown in Figure 3.18 using V_{DS} = 0.1 V. It is seen that the InGaZnO (1:1:5) exhibit a higher mobility and a lower S than the (1:1:1) devices. Since this drain voltage bias represents the linear region of operation, the definition for V_{TH} used here is the gate voltage at which I_D = 1 nA. Five devices with W/L = 100 µm/10 µm = 10 were measured from each batch for statistical confirmation of

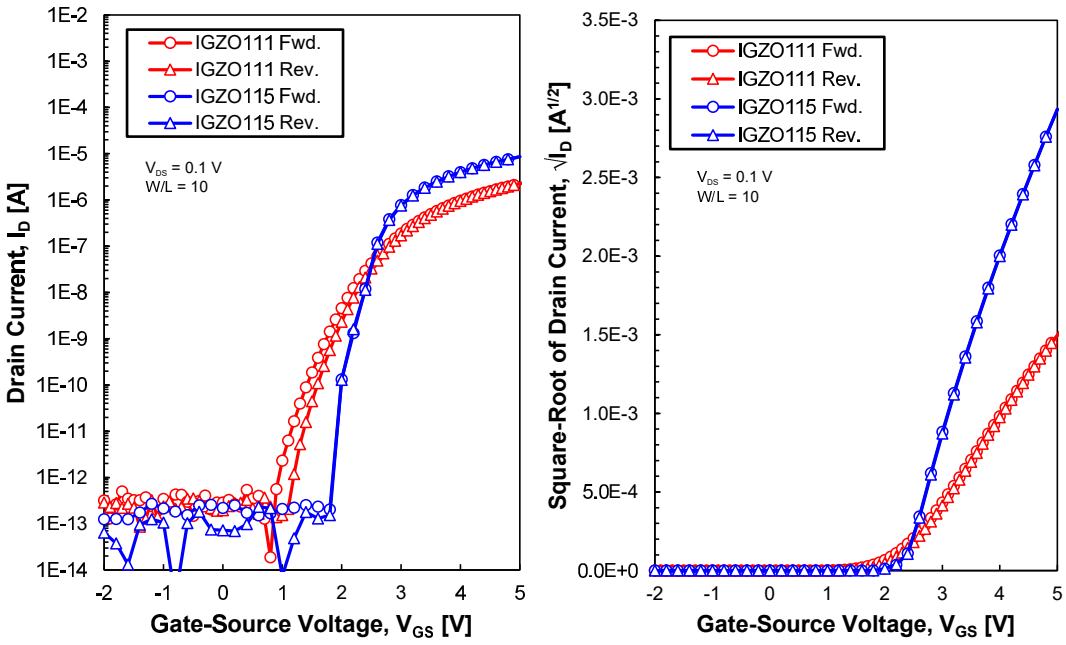


Figure 3.18. Comparison of (a) $I_D - V_{GS}$ and (b) $\sqrt{I_D} - V_{GS}$ between PLD-InGaZnO (1:1:1) and PLD-InGaZnO (1:1:5) Generation 3 TFTs with W/L = 10 (V_{DS} = 0.1 V).

performance. For the (1:1:1) devices: V_{TH} = 2.1 ± 0.3 V, $\mu_{FE,LIN}$ = 3.9 ± 1.1 $cm^2\ V^{-1}\ s^{-1}$ and S = 304 ± 79 mV/dec. For the (1:1:5) devices: V_{TH} = 2.2 ± 0.3 V, $\mu_{FE,LIN}$ = 14.1 ± 1.8 $cm^2\ V^{-1}\ s^{-1}$ and S = 167 ± 42.1 mV/dec. Though these values were obtained in the linear region (V_{DS} = 0.1 V), they can be compared to a first-degree with the previously cited report on ALD Al_2O_3/RF-sputtered InGaZnO TFTs [142], whose performance at V_{DS} = 5 V was V_{TH} = 0.4 ± 0.1 V, $\mu_{FE,SAT}$ = 8 ± 1 $cm^2\ V^{-1}\ s^{-1}$, an on/off ratio of 10^7 and sub-threshold swing of 100 ± 10 mv/dec. Both of the PLD InGaZnO compositions yield TFTs with larger V_{TH} and S. However, the on/off ratio is the same order of magnitude, while the InGaZnO (1:1:5) TFTs are characterized by a larger mobility.

3.5.3 Intrinsic Performance Extraction via Transfer Length Method

In 3.2, it can be seen that there is a reduction in μ_{SAT} in the TFTs with larger W/L ratio. This dependence on geometry arises due to the presence of contact resistance, R_c, between the S/D metal and the InGaZnO layer that cannot be completely ignored. To investigate this effect in more detail, Generation 3 devices with different W/L ratios were also compared

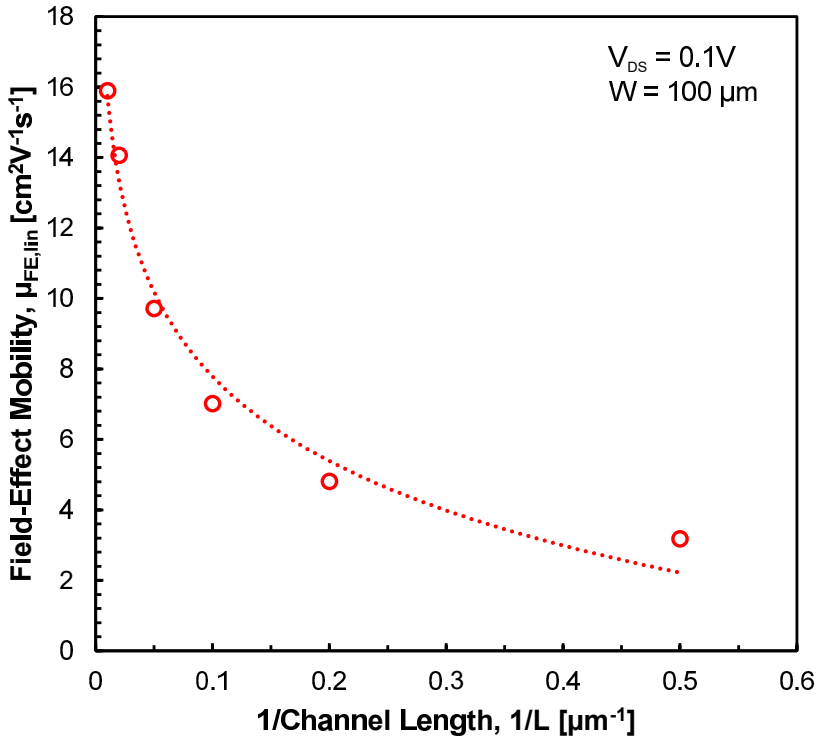


Figure 3.19. Change of the field-effect mobility with respect to the inverse of the channel length. Measured in the linear regime (V_{DS} = 0.1 V).

against each other. Each TFT had constant W = 100 µm but varying lengths, L = 2, 5, 10, 20, 50, 100 µm. The TFTs in this experimental set were fabricated using 50 nm thick ALD Al_2O_3 deposited at GT at 180 °C (i.e., the same films as those analyzed in Section 3.4.1), 50 nm thick PLD InGaZnO (1:1:5), and, unlike the devices presented in Figure 3.18, used individual Cr/Au gates (see Figure 3.8). The degradation of $\mu_{FE,LIN}$ has been plotted against 1/L (∝W/L) in Figure 3.19.

The field-effect mobility, calculated based on the equations in Section 2.2.3 is, in fact, an extrinsic representation of the device performance. The intrinsic performance can be obtained through the transfer length method (TLM) as follows [124]. Firstly, for any given bias point, it is possible to calculate the total ON resistance of the channel (R_T):

$$R_T = \frac{V_{DS}}{I_D} = R_{c,S} + R_{c,D} + R_{ch} = 2R_c + r_{ch}L \tag{3.4}$$

where $R_{c,S}$ and $R_{c,D}$ are the contact resistances at the Source and Drain contacts, respectively, R_{ch} is the channel resistance and r_{ch} is the semiconductor channel's resistance per unit length. Using Equation 2.11, this can be rewritten as

$$R_T = \frac{L}{WC_i\mu(V_{GS} - V_{TH})} \tag{3.5}$$

The dependence of R_T on both L and V_{GS} is shown in Figure 3.20. As expected, R_T increases linearly with L. Moreover, as V_{GS} increases further and further above V_{TH}, the accumulation of charge carriers becomes more prominent, causing R_T to decrease. From Equation 3.4, when L=0 (i.e., y-intercept of R_T (L)), $R_T = 2R_c$. Additionally, the slope of R_T (L) yields r_{ch} . Therefore, Figure 3.20 can be used to extract the V_{GS}-dependent values of R_c and r_{ch} in the TFT. These results are summarized in Figure 3.21, where it can be seen that the contact resistance is on the same order of magnitude as the channel resistance itself. This is not a desirable performance trait, and further investigations into metalization schemes for IGZO (1:1:5) need to be developed to lower R_c. Possible methods of doing this include reducing the Cr thickness from 25 nm to ≤10 nm [165] or using Ti instead of Cr as the adhesive layer [142, 166].

From Equation 3.2, it is known that L_T is somehow dependent on R_c, and therefore it should be possible to quantify the value of L_T for these devices. To do this, Equation 3.4 needs to be adjusted:

$$R_T = 2R_C + R_{SH}\frac{W}{L} \tag{3.6}$$

where

$$R_C = \rho_c\frac{1}{WL_T} = \frac{R_{SH}L_T}{W} \tag{3.7}$$

and therefore

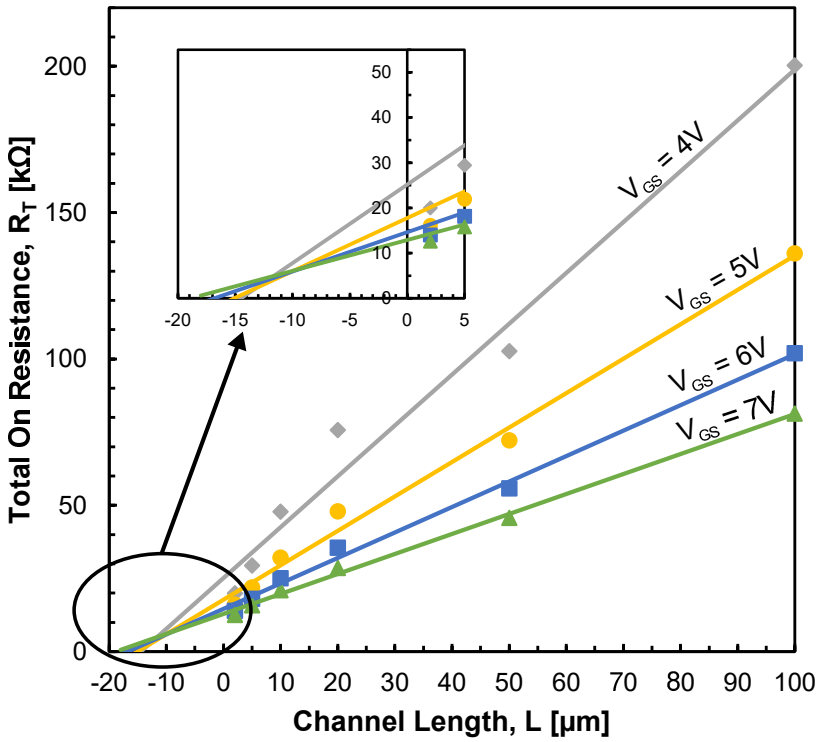


Figure 3.20. Total ON resistance versus the channel length (L) for various V_{GS} values. The resistance decreases as V_{GS} increases due to the enhanced degree of accumulation (V_{DS} = 0.1 V).

$$R_T = \frac{2R_{SH}L_T}{W} + R_{SH}\frac{W}{L} = (L + 2L_T)\frac{R_{SH}}{W} \tag{3.8}$$

As a result, the x-axis intercept of Figure 3.20 yields the value $2L_T$. For these TFTs, 7.2 μm ≤ L_T ≤ 9.4 μm, which means that nearly the entire contact is active ($L_T \sim L_c$). For good contacts, typical L_T values are ≤1 μm. Though this behavior is not desirable, it is not critical for sensor applications investigated in this thesis. In the future, efforts should be allocated to reducing R_c and L_T so that the same devices can be used for both chemical sensing as well as active circuitry.

Lastly, TLM can also be used to extract the intrinsic mobility (μ_i) and intrinsic threshold voltage ($V_{TH,i}$). This can be obtained by neglecting the effect of the contact resistances:

$$\frac{1}{r_{ch}} = WC_i\mu_i\,(V_{GS} - V_{TH,i}) \tag{3.9}$$

This data is plotted in Figure 3.22. The x-axis intercept provides $V_{TH,i}$ = 1.91 V, while

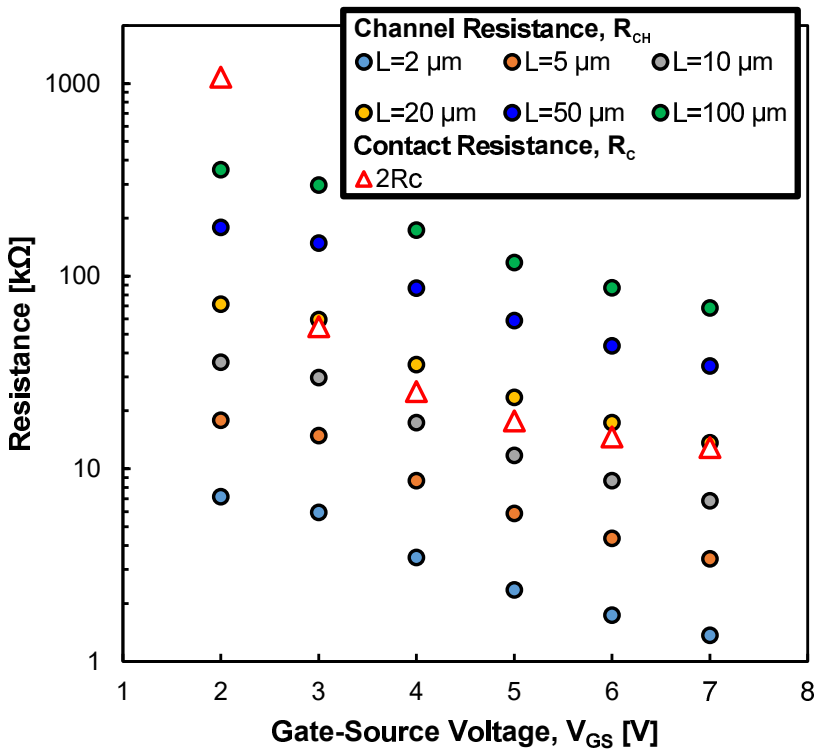


Figure 3.21. Channel and contact resistances plotted as a function of V_{GS} (V_{DS} = 0.1V).

the slope reveals that μ_i = 17.8 cm^2 V^{-1} s^{-1}. This value can then be compared with the values in Figure 3.19 where, as $1/L \rightarrow 0$, $\mu_{FE,lin} \rightarrow \mu_i$. The intrinsic mobility observed in these TFTs is on par with previously reported InGaZnO TFTs from the literature (Section 3.1), and indicates satisfactory TFT operation and performance for chemical sensing devices.

3.6 Conclusion

This chapter has described issues of device and die-level layout in the context of improving device performance, as well as facilitating the deployment of InGaZnO TFTs as chemical sensors. An overview of the low-temperature microfabrication processes has been provided, with particular emphasis being placed on the gate dielectric deposition using atomic layer deposition and deposition of InGaZnO using RF sputtering or pulsed laser deposition (PLD). Generation 2 RF-sputtered InGaZnO TFTs exhibit a typical performance of V_{TH} = 4 V, S = 270 mV/dec, $I_{ON/OFF} \sim 10^{10}$ and, for a W/L ratio of 106, $\mu_{FE,SAT}$=5.3 cm^2 V^{-1} s^{-1}. This is compared to Generation 2 PLD InGaZnO (1:1:1)-based TFTs that showed V_{TH} =

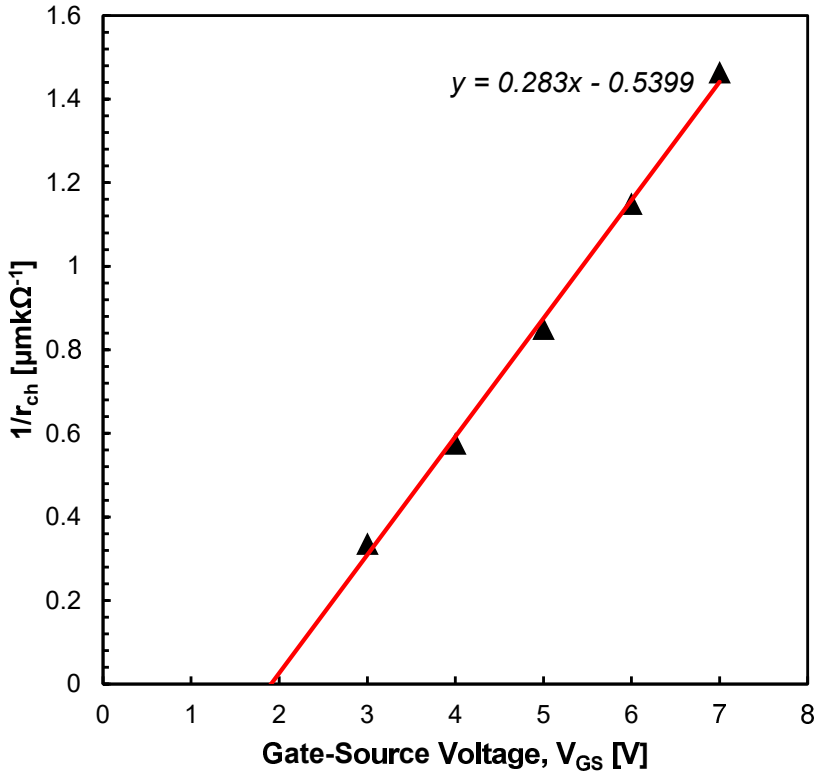


Figure 3.22. Inverse of the channel resistance per unit length versus V_{GS} (V_{DS} = 0.1V).

1.4 V, S = 230 mV/dec, $I_{ON/OFF} \sim 10^9$ and, for a W/L ratio of 106, $\mu_{FE,SAT} = 6.6\ cm^2\ V^{-1}\ s^{-1}$. Statistical analysis conducted on Generation 3 TFTs with PLD InGaZnO (1:1:1) and PLD InGaZnO (1:1:5) revealed that InGaZnO (1:1:5) TFTs achieved better performance, namely $V_{TH} = 2.2 \pm 0.3$ V, $\mu_{FE,LIN} = 14.1 \pm 1.8\ cm^2\ V^{-1}\ s^{-1}$ and S = 167 ± 42.1 mV/dec. Finally, the transfer length method was used to extract the intrinsic performance of TFTs made with PLD InGaZnO (1:1:5). This process shed light on the major impact of the W/L ratio on the extrinsic μ_{FE}, unveiling that $\mu_i = 17.8\ cm^2\ V^{-1}\ s^{-1}$. This value compares favorably with previously reported results and offers sufficient validation of performance to pursue chemical sensing applications. Future efforts should be directed towards lowering the contact resistance, as well as the threshold voltage for low-power operation.

CHAPTER 4

PULSED OPERATION OF InGaZnO TFTS FOR VOC SENSING APPLICATIONS

The detection of volatile organic compounds (VOCs) using InGaZnO TFTs operating at room temperature is explored. Pulse-mode biasing to improve the long-term stability of these TFTs when exposed to the environment and under bias stress is proposed. Coated with a non-conducting polyepichlorohydrin (PECH) film, the TFTs under constant voltage bias exhibit a reversible response to varying ethanol concentrations in the gas phase. Furthermore, by lowering the duty cycle (δ) using bias pulses, the drain current decay under voltage bias can be reduced, thus extending the device's operational lifetime while simultaneously lowering power consumption for mobile applications.

4.1 Prior Art

The most straightforward implementation of an InGaZnO-based gas-phase chemical sensor is the chemiresistor. Metal oxide chemical sensors of this type have a long history [167, 168], and rely on changes in resistance due to reduction and oxidation reactions at the gas/thin film interface. Though these sensors show stable performance and high sensitivity to certain gases, they depend on either high temperature operation [71], or high temperature thin film deposition [72]. This makes it difficult to implement these devices on flexible substrates, or operate them in a portable/body-wearable platform. Chemically-sensitive FET structures have also been investigated for chemical sensing. In its simplest form, the top-gate metal contact of a Si CMOS device is made of palladium (Pd) [169]. In this case, hydrogen is able to diffuse through the Pd gate and causes a change in the work function at the Pd-SiO_2 interface. This, in turn, brings about a measurable shift in the device's threshold voltage (V_{TH}). Similar devices have been realized using InGaZnO TFTs [170, 171], where a separate Pd-based capacitor is connected to the gate contact of the

transistor.

The above approaches utilize top-gate devices, whereas the most common TFT structure is an inverted, or bottom-gate structure. Moreover, the use of an off-chip Pd-capacitor adds an extra degree of complexity to the system. Thus far, only one example of a bottom-gate InGaZnO TFT gas sensor exists [73]. In that work, the bare TFT did not exhibit a response to 0.1-5 ppm concentrations of ammonia or acetone, but, when exposed to 50-100 ppm of nitric oxide (NO), the current was observed to reduce without signs of recovery during the purge cycles. The TFT was then capped with semiconducting organic polymers poly(3-hexylthiophene) (P3HT) and copper phthalocyanine (CuPc) to enhance sensitivity, making it possible to observe a response to all three analytes. However, there exist several examples in the literature that demonstrate that conductive or semiconducting polymers exhibit their own sensitivity to such gases [74–76]. Therefore, it is unclear to what degree the InGaZnO TFT contributes to the sensing performance in this system. The authors of [73] argued that organic sensing layers act as a second gate of the device, thereby capacitively coupling into the InGaZnO channel.

A further concern for any sensor is baseline drift, which can affect both the reliability and accuracy of the device's response. In all of the above scenarios, the TFTs are operated under a constant voltage bias and the corresponding drain current is monitored in the presence of VOCs. As with both metal oxide semiconductor TFTs, as well as TFTs made with more traditional technologies, such as α-Si:H [172], it has been widely shown that InGaZnO TFTs suffer from constant bias stress instability that causes I_D to decay exponentially over time [173, 174]. Many strategies have been put forth to mitigate this effect, such as high-temperature post-process wet annealing [162], the deposition of passivation layers [83] to protect the active layer, and the use of AC/pulsed biasing [175, 176]. Nonetheless, much work is still required before true stability is reached. For this reason, it is proposed that a combination of fabrication and system-level strategies, namely post-process annealing and reduction of the duty cycle (δ) through pulsed operation, can be used to improve

the baseline stability of InGaZnO TFT-based chemical sensors. Using these techniques in tandem, it is found that the shift in the threshold voltage (ΔV_{TH}) and, as a result, the change in the drain current (δI_D) under constant voltage bias can both be significantly reduced and effectively controlled. Thus, the response of a bare bottom-gate InGaZnO TFT to ethanol is presented for both δ =100% and δ =10%. In addition, the backside of the device is coated with a non-conducting polymer, which is known to sorb ethanol and gave rise to a boost in the sensor's response.

4.2 Fabrication and DC I-V Characterization of InGaZnO TFTs

The InGaZnO TFTs used in this study use the second generation (inter-digitated) design described in Chapter 3. They consist of a 200 nm Al bottom gate, 50 nm Al_2O_3 gate dielectric layer obtained via ALD at 180 °C, RF sputtered InGaZnO (1:1:1) active layer of 50 nm thickness and 25/200 nm Cr/Au S/D contacts. The electrical performance of the TFT can be extracted from a typical transfer characteristic (I_D vs. V_{GS}) shown in Figure 4.1. A linear extrapolation of the square-root of I_D as a function of V_{GS} in the saturation region (dashed line) shows that the threshold voltage is ~ 1.9 V. Additionally, it is observed that the on/off ratio is > 10^7, μ_{SAT} is ~4 $cm^2V^{-1}s^{-1}$ and the sub-threshold swing, S, is 180 mV/dec.

4.3 Bias Stress Management

In order for the InGaZnO TFT to be deployed as a sensor, it is imperative that the issue of bias stress instability be addressed. From our own measurements, as well as from those published in the literature [73, 177], it has been observed that a steady I_D cannot be maintained over time at a constant bias point defined by fixed positive V_{GS} and V_{DS}. Instead, the current decay that is recorded under these conditions follows a stretched exponential function. It has been proposed [10] that this stretched exponential behavior, which is also seen in Si field-effect transistors (FETs) with high-k [178] and SiN_x gate dielectric [172] is

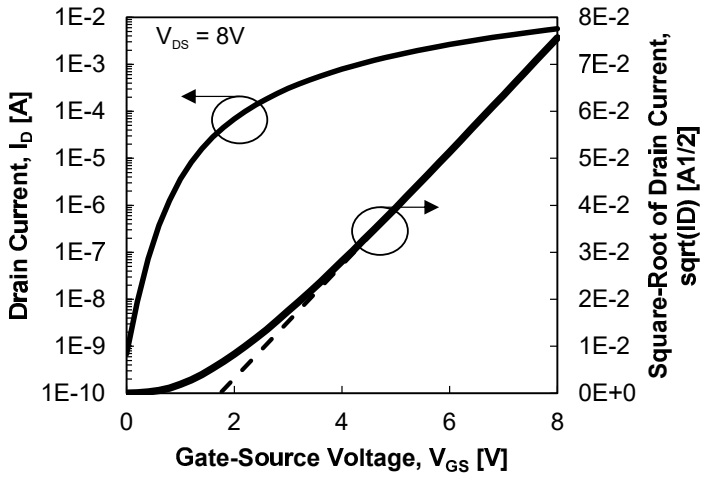


Figure 4.1. Transfer characteristic of a TFT with a 5μm channel length (V_{DS} = 8 V). I_D is plotted on a log scale on the left, while the square root of I_D is plotted on the right.

explained by the presence of charge trapping states at the interface between the dielectric and active layers, or within the active layer itself. When the TFT is on, electrons traveling in the channel along this interface are captured by these traps and act against the externally applied electric field at the gate, resulting in an effective increase of V_{TH}. The change in V_{TH} is described by the following equation [173]:

$$V_{TH}(t) = V_{TH,0}\left(1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right) \tag{4.1}$$

where $V_{TH,0}$ represents the value of V_{TH} as time, t, tends to infinity, τ is the characteristic trapping time of the carriers that is dependent on the activation energy $\tau = \tau_0 \exp(E_a/kT)$ of the trap and β is a constant related to the energy barrier presented by the dielectric at the interface. Therefore, for an ideal TFT with $\Delta V_{TH}(t \to \infty) = 0$, $\tau \to \infty$.

To investigate whether the semiconductor-insulator interface is, at least partially, the source of the threshold voltage shift due to bias stress, C-V measurements were conducted on a 100×100 μm^2 MIS structure before and after stress. As is observed in Figure 4.2, the capacitance begins to increase when a DC voltage of 1.2 V is applied to the pre-stressed device. After 60 minutes of bias stress (V_{DC} = +5 V), the turn-on voltage shifts to the right, showing the onset of capacitance increase (i.e., accumulation) when V_{DC} >2V. This

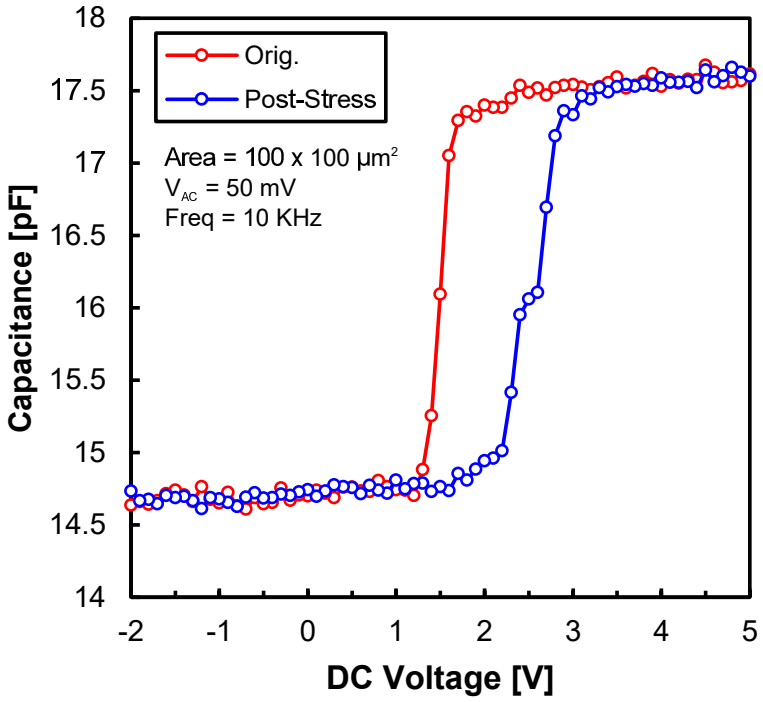


Figure 4.2. Bias stress measurement (+5V) conducted on MIS structure for 60 minutes, showing a noticeable shift in C-V characteristic.

result confirms that the semiconductor-insulator interface does indeed contribute to ΔV_{TH} in InGaZnO TFTs as a result of positive bias stress (PBS).

In an effort to minimize ΔV_{TH}, post-process annealing and pulse-mode operation are proposed. Each technique was evaluated by monitoring the ΔV_{TH} of TFTs with channel lengths of 10 μm and a W:L ratio of 106 over a period of 30 min while applying $V_{GS} = V_{DS} = 8$ V. Instantaneous values for V_{TH} were extracted from I_D vs. V_{GS} sweeps that were conducted every 5 minutes throughout the stress test. The measurements were carried out in a sealed metal case (i.e., no light) in air at room temperature and with a Keithley Instruments Inc. 2636A low-current dual-channel sourcemeter. To ensure repeatability, multiple devices on the same die were tested for each condition and the average values are presented below.

4.3.1 Post-Process Annealing

It has been found that a simple, yet effective method for increasing the stability of the TFT is to use a post-process anneal in air [179, 180]. In this work, the anneal time was kept

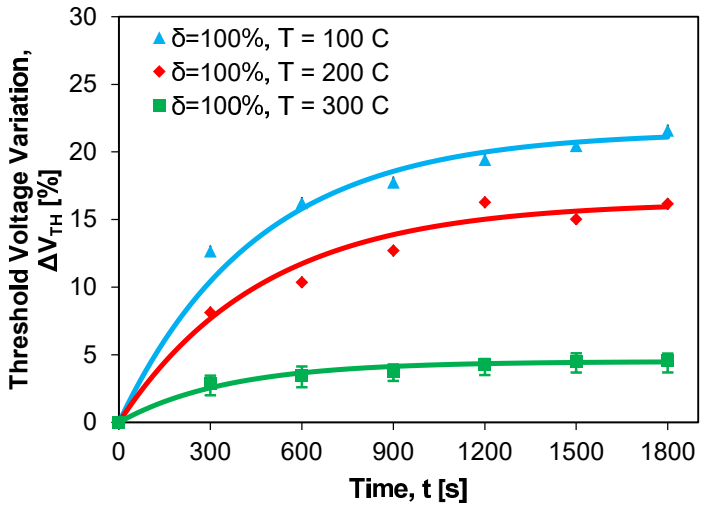


Figure 4.3. Relative change of the threshold voltage, ΔV_{TH}, as a function of bias time for a bias stress of $V_{GS} = V_{DS} = 8$ V. The trends for devices with L = 10 μm annealed for 90 minutes in air at temperatures of 100 °C, 200 °C and 300 °C are shown. The duty cycle is maintained at 100%. The data are described by stretched-exponential functions (see Equation 4.1).

constant at 90 minutes while three different annealing temperatures were investigated: 100 °C, 200 °C and 300 °C. The averaged threshold voltage shifts vs. time are presented in Figure 4.3 with error bars to show the measurement variance.

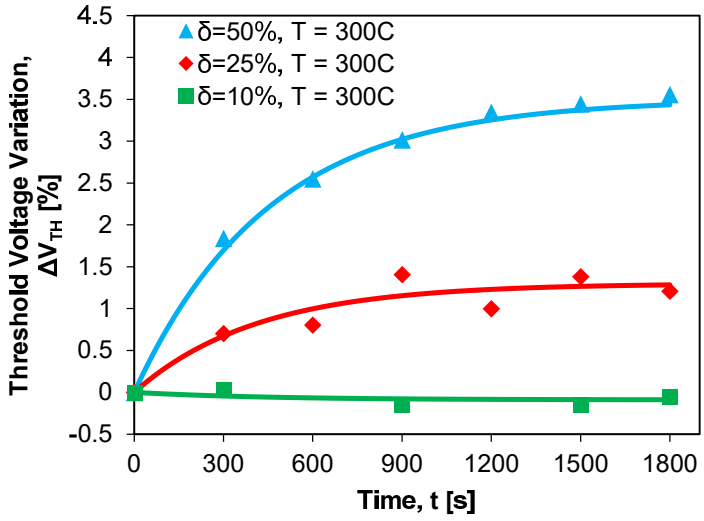
A clear dependence on the annealing temperature is observed and indicates that higher temperatures are required to achieve better stability. For the investigated devices, higher temperature annealing also results in significantly smaller performance variability from device to device (shown in Figure 3 are only the error bars for devices annealed at 300 °C). It is believed that annealing reduces the number of subgap states as well as the number of oxygen vacancies in the active layer in order to produce a more stable device [162]. However, from our own electrical characterization measurements, a decrease in V_{TH} was recorded with respect to the original (not annealed) device. Thus, it is possible that annealing may also lead to a reduction in the number of interfacial charge traps and, therefore, their ability to affect device stability under constant bias stress.

4.3.2 Pulsed Operation via Duty Cycle Control

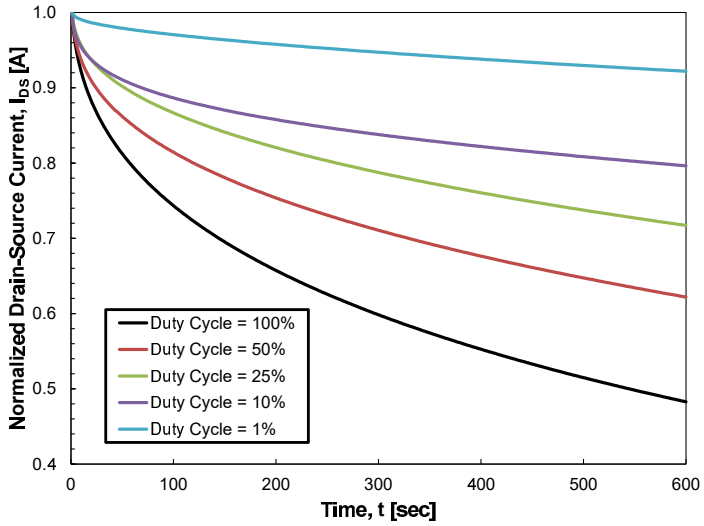
Though the reduction of ΔV_{TH} to approximately 5% after 30 min (from Figure 4.3) may seem sufficient, this metric is, in actuality, misleading for a sensor application because the corresponding change in I_D at the bias point is still $\delta I_D \sim$ -40%. This degree of instability in a sensor's baseline generally cannot be tolerated. As such, the reduction of the duty cycle, δ, via pulsed operation of the TFT was investigated and is presented in Figure 4.4 for δ = 50%, 25% and 10%.

It is apparent that adjustment of the duty cycle (δ) translates into better control of ΔV_{TH}. For example, when δ = 25%, $\Delta V_{TH} \sim 1\%$ or $\delta I_D < -7\%$. Moreover, it is observed that with a low enough duty cycle, e.g. δ = 10%, it may be possible to reverse the trend altogether such that ΔV_{TH} becomes negative. This behavior suggests that an optimum duty cycle may be identified for each device, with which a reference I_D can be reliably defined throughout the TFT sensor's deployment.

These results differ from previously reported studies on the use of pulsed or AC biasing. It was previously found that for a fixed duty cycle of 50%, increasing the frequency from 100 Hz to 1 MHz decreased ΔV_{TH} [175]. In that study, V_{DS} = 0 V during V_{GS} pulsing. However, another study reported that the application of δ=50% pulses to V_{GS} during stress while V_{DS} = 0 V increased ΔV_{TH} compared to the case where a constant V_{GS} was used [156]. The same group then published another study of pulsed biasing, this time applying V_{DS} = 15 V during the stress periods [176]. Under these new bias conditions, it was found that pulsing does, in fact, reduce ΔV_{TH}. The difference between the two findings was attributed to the addition of self-heating when V_{DS} is applied. However, unlike the measurements presented in this thesis, the authors of [176] claimed that variation of δ cannot be used to control ΔV_{TH}. Therefore, this work shows for the first time that δ reduction can indeed be leveraged to improve positive bias stress stability. The reasons for this difference need to be studied in more detail, and could be due to differences in device geometry as well as contact resistance, particularly if self-heating is a major determinant of stability.



(a)



(b)

Figure 4.4. Relative change of (a) the threshold voltage (ΔV_{TH}) and (b) normalized the drain current (I_d) as a function of bias time for a bias stress of $V_{GS} = V_{DS} = 8$ V. The trends for devices with L = 10 μm annealed for 90 minutes in air at a temperature of 300 °C but with varying duty cycles during bias stress are shown. The data are fitted by stretched-exponential functions (see Equation 4.1).

A further favorable consequence of utilizing lower duty cycles lies in power management. Since the device can be turned off for the majority of each cycle, less average energy is consumed, thus potentially paving the way for battery-operated or autonomous sensors based on this technology.

4.4 VOC Sensing

This section examines the response of InGaZnO TFTs to various concentrations of ethanol, which is an example of a typical VOC. Throughout the measurements, the TFTs were operated at room temperature. This is in stark contrast to other sensor architectures, such as chemo-resistors based on metal oxides or other materials that need to be operated at elevated temperatures (> 200 °C) [71]. Mass-flow controllers (MFCs) were used to regulate the concentration of the analyte. Following each analyte exposure, a purge cycle was executed by flowing synthetic air (20% O_2 and 80% N_2) over the device.

Figure 4.5 depicts the typical response of a bare TFT biased in the saturation region with $V_{GS} = V_{DS} = 8$ V and $\delta = 100\%$. The sensor shows a significant decay in I_D during the windows of ethanol exposure, followed by an increase in current during the purge cycles. For example, 25500 ppm of ethanol induced a downward δI_D of 0.5-0.6 μA or 5-6%. The average sensitivity is thus calculated to be 19 pA/ppm. The lack of complete saturation following the 3 min ethanol exposure indicates that the time constants are large, and could pose a challenge to these sensors when compared to competitors, such as mass-sensitive resonant cantilevers [181]. Though the drain current does entirely flatten out, the downward slope is attributed to the presence of baseline drift from positive bias stress, as shown in Figure 4.4b. Likewise, the purge time constants also appear to be large, and could be affected by baseline drift. It should be noted that this result is in contrast to the results in [73], since the bare TFT's current is able to recover.

A common technique for improving the sensitivity of VOC sensors involves the use of organic polymers capable of absorbing the analyte of interest. In this work, we use polyepichlorohydrin (PECH) as it is known to adsorb ethanol [181, 182]. Unlike the polymers that have been investigated in [73], which are conducting in nature, PECH is non-conducting. In this way, any fluctuation in I_D must occur in the InGaZnO film itself. The response of the PECH-coated device, which was biased in the same manner as the bare device's, is shown in Figure 4.7. Two main differences in the sensor response can be seen:

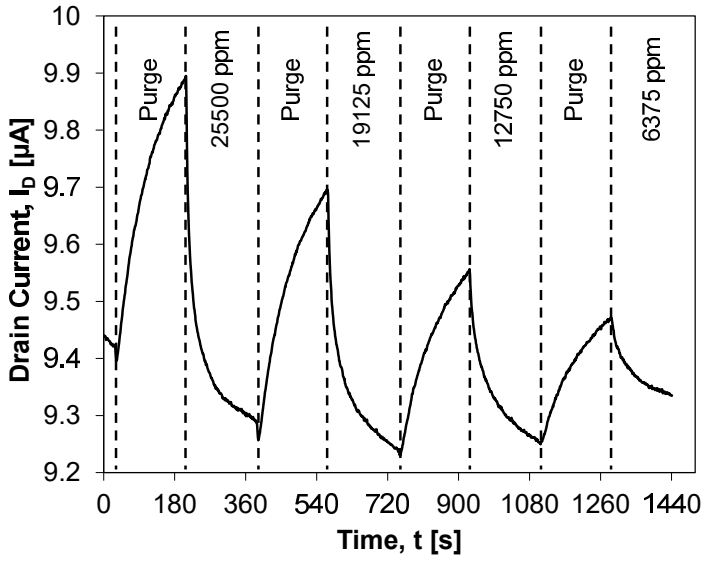


Figure 4.5. Drain-current vs. time under constant bias conditions (V_{GS} = V_{DS} = 8 V) for a bare InGaZnO TFT subjected to consecutive ethanol exposures of varying concentrations and synthetic air purges.

(1) the polarity of the response is inverted such that the presence of ethanol now causes a rise in I_D and (2) the amplitude of the response is increased. For 25500 ppm, a δI_D of approximately 2 μA (or 15%) is recorded, which represents a 3-4 fold amplification of the response, or an average sensitivity of 78 pA/ppm. In addition to these characteristics, it is observed that before the overall rise in current is observed for each ethanol exposure, there exists a short and rapid drop in current. The time constant of this current reduction is very small, and is in contrast to the large time constant of the subsequent current rise. Similar effects are also seen during the purge periods.

While more investigation is required to fully understand the sensing mechanisms at play for both the bare and PECH-coated TFTs, some potential explanations are considered here. Firstly, it is well known that at room temperature, the V_{TH} of bare InGaZnO TFTs can be affected by exposure to oxygen or water [84, 140]. In this case, oxygen is donated to the InGaZnO, filling oxygen vacancies and, in turn, accepting free carriers, which increases V_{TH} and reduces mobility. It is possible that the exposure of a bare InGaZnO TFT to ethanol induces a similar effect, and therefore accounts for the decrease in I_D that is observed. In this case, oxygen donation by the ethanol would have to be of a shallow

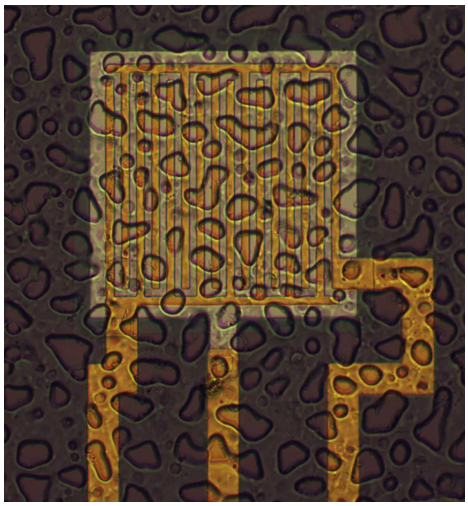


Figure 4.6. Top-view photograph of InGaZnO TFT with spray-coated PECH sensing layer.

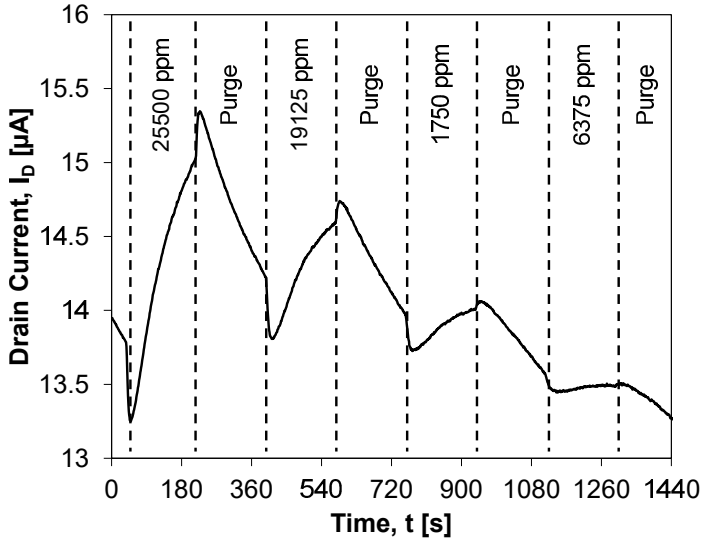


Figure 4.7. Drain-current vs. time under constant bias conditions (V_{GS} = V_{DS} = 8 V) for a PECH-coated InGaZnO TFT subjected to consecutive ethanol exposures of varying concentrations and synthetic air purges.

nature in order to permit current recovery during the purge cycles. To explain the change in response with the addition to PECH, Dutta et al. [183] proposed that ethanol's polar molecules may trap any holes in the organic film and consequently screen the V_{GS} bias. Since their pentacene/InGaZnO TFT possessed V_{TH} <0, this corresponded to an increase in drain current. The TFTs in this thesis are enhancement mode devices and therefore a reduction in current would be expected according to this explanation. An increase in I_D, however, could be explained by the accumulation of dipole charge in the PECH that causes

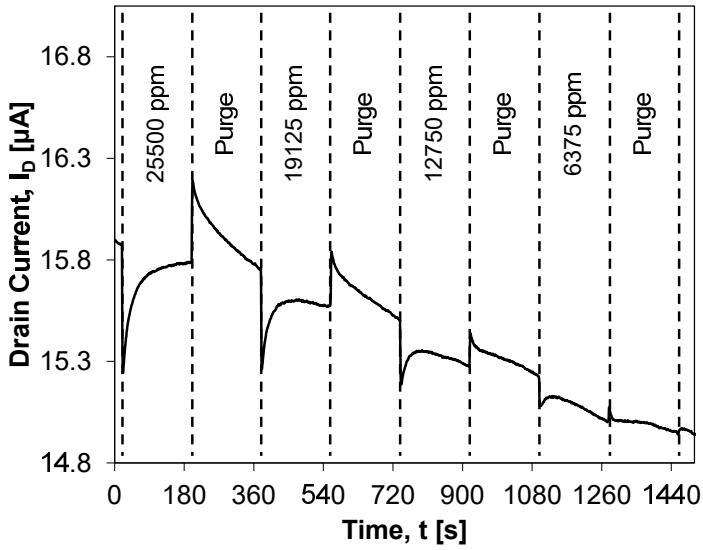


Figure 4.8. Drain-current vs. time under constant bias ($V_{GS} = V_{DS} = 8$ V) stress with $\delta = 10\%$. A bare InGaZnO TFT is subjected to consecutive ethanol exposures and synthetic air purges.

an accumulation of carriers in the InGaZnO too. The short current spikes that arise in the PECH-coated TFT's response could be attributed to non-uniformity of the spray-coated PECH layer, which allows the bare TFT's response (with a short time constant) to dominate initially, before being overshadowed by the PECH layer's amplified effect. To overcome this effect, the introduction of an ultra-thin and electrically insulating barrier film below the PECH could prevent direct InGaZnO-ethanol interaction and permit the study dipole charge coupling into the InGaZnO instead.

Lastly, the response of a bare TFT to ethanol while operating with $\delta = 10\%$ was investigated. The result (Figure 4.8), though different to what was observed when $\delta = 100\%$, still shows changes in I_D that are proportional to the ethanol concentration. Interestingly, the response is very similar to the PECH-coated TFT's response, in that ethanol produces an initial reduction in current before subsequently increasing. However, the observed time constant appears to be shorter than that seen in the PECH-coated case. It is believed that the existence of these fast transients indicates the possibility of competing sensing mechanisms, each with different time constants. One possibility, which requires confirmation, is that the voltage bias applied to the TFT affects the ethanol adsorption. For example,

the bottom gate contact is only separated from the InGaZnO-air interface by 100 nm, and would therefore allow some degree of capacitive coupling across the structure. During pulsing, the effective DC bias of the TFT is reduced, and the ethanol could be repelled (or less favorably adsorbed) during the OFF portions of the pulse. To study this effect, the bare TFT's response to ethanol could be studied with δ = 100% at different bias points.

4.5 Conclusions

The application of amorphous InGaZnO TFTs to VOC sensing has been explored. Firstly, the issues of electrical instability that arises from bias stress have been investigated. Thermal annealing, which has been widely shown to improve TFT performance in the literature, has been coupled with pulse-mode biasing. Whereas other groups had previously proposed pulsed biasing, their studies had focused on varying the pulse period rather than the duty cycle. In this work it is shown that for a fixed period, the reduction of the duty cycle can also reduce ΔV_{TH}. Specifically, use of a 25% duty cycle reduced the drift to <1.5%; when a duty cycle of 10% was used, the drift came down to <0.5%. These techniques were applied to investigate the ability of InGaZnO TFTs to be used for gas-phase VOC sensing, in particular with ethanol. Concentrations of 6375 to 25500 ppm were detected by bare devices, with an average sensitivity of 19 pA/ppm. The addition of an insulating PECH polymer layer on top of the InGaZnO channel increased sensitivity by 3-4x, resulting in a maximum sensitivity of 78 pA/ppm. Though potential explanations have been provided for the sensing response in each case, further studies need to be carried out. These should focus on understanding the changes in response polarity between the bare and PECH-coated devices, as well as what factors influence the time constants of the response.

CHAPTER 5

PASSIVATION OF $InGaZnO_{115}$ THIN FILM TRANSISTORS USING ATOMIC LAYER DEPOSITION OF TIO_X

In this chapter, the issue of thin film passivation of InGaZnO TFTs is studied. Passivation is an essential fabrication step for these devices, as it improves their stability due to bias and environmental effects, as well as permits them to operate in liquid for liquid-phase sensing applications. The challenges associated with thin film passivation are discussed, leading to a systematic study of the suitability of atomic layer deposited (ALD) titanium oxide (TiO_x) for passivation of $InGaZnO_{115}$ TFTs. It is found that the passivated TFTs' behavior depends on the TiO_x deposition temperature, affecting device characteristics such as threshold voltage (V_{TH}), field-effect mobility (μ_{FE}) and sub-threshold swing (S). An O_2 annealing step is required to recover TFT performance after passivation. It is also observed that the positive bias stress (PBS) response of the passivated TFTs improves compared the original bare device. Secondary ion mass spectroscopy (SIMS) excludes the effects of hydrogen doping and inter-diffusion as sources of the temperature-dependent performance change. Instead, it is proposed that oxygen gettering induced by TiO_x passivation creates oxygen vacancies in the InGaZnO film.

5.1 Introduction

It has been observed that defects, such as oxygen vacancies and charge traps, can affect the performance of InGaZnO TFTs. Dry and wet annealing have been found to reduce defect densities at the dielectric-semiconductor interface and in the semiconductor bulk itself, in turn improving bias and illumination stress stability. [162, 184] For bottom-gate TFTs, the exposed semiconductor surface at the top is also a potential source of instability, which has prompted numerous studies of passivation strategies. The most successful of these have focused on the use of organic materials that can be deposited at room temperature

under atmospheric conditions (e.g., spin-coating). [84, 185, 186] Such films have proven to reduce the TFT's sensitivity to both atmospheric oxygen content, as well as bias stress stability (introduced in Section 4.3). Inorganic materials, such as SiO_2 [139] and Al_2O_3 [187], have also been studied.

In general, it has been found that unintentional H_2 doping and/or plasma damage arising from thin film deposition can have major effects on the passivated TFT's performance, often leading to large negative shifts in V_{TH} or low on/off ratios [85]. Examples of these effects have also been observed in-house for a variety of inorganic passivation film materials and deposition methods using the InGaZnO TFTs made with the Generation 2 mask set. In Figures 5.1a and 5.1b, atomic layer deposition at 180 °C of Al_2O_3 and a nanolaminate stack-up of ZrO_2/Al_2O_3 were used as passivation. In both cases, the devices became highly conductive, even after a post-passivation annealing step. Plasma-enhanced chemical vapor deposition of SiN_x was also investigated as a passivation film (see Figure 5.1c), and similar effects were also seen. However, when an organic polymer, such as parylene, was used the transistor characteristic of the TFT was preserved, showing only a small positive shift in V_{TH} post-passivation (Figure 5.1d).

In this chapter, a particular focus is placed on the use of TiO_x deposited by atomic layer deposition (ALD) as a passivation layer. TiO_x has emerged as an attractive moisture barrier film [188] that has been employed to stabilize organic TFTs [189], slow down corrosion in photoelectrochemical cells [190] and permit high-sensitivity chemical sensing. [191] In the context of InGaZnO TFTs, the temperature-effect of TiO_x passivations has not been systematically studied and has resulted in a number of conflicting reports. Seo et al. [192] deployed an oxygen plasma step to oxidize sputtered Ti on the top surface of the InGaZnO film. The threshold voltage (V_{TH}) remained unchanged as a result of this treatment, while the field-effect mobility (μ_{FE}) increased and drift in threshold voltage ($V_{TH,NBS}$) due to negative bias stress (NBS) was reduced compared to the bare TFT. On the other hand, Wu et al. [193] sputtered TiO_2 and observed significant increases to both μ_{FE} (+1.16 $cm^2\,V^{-1}\,s^{-1}$)

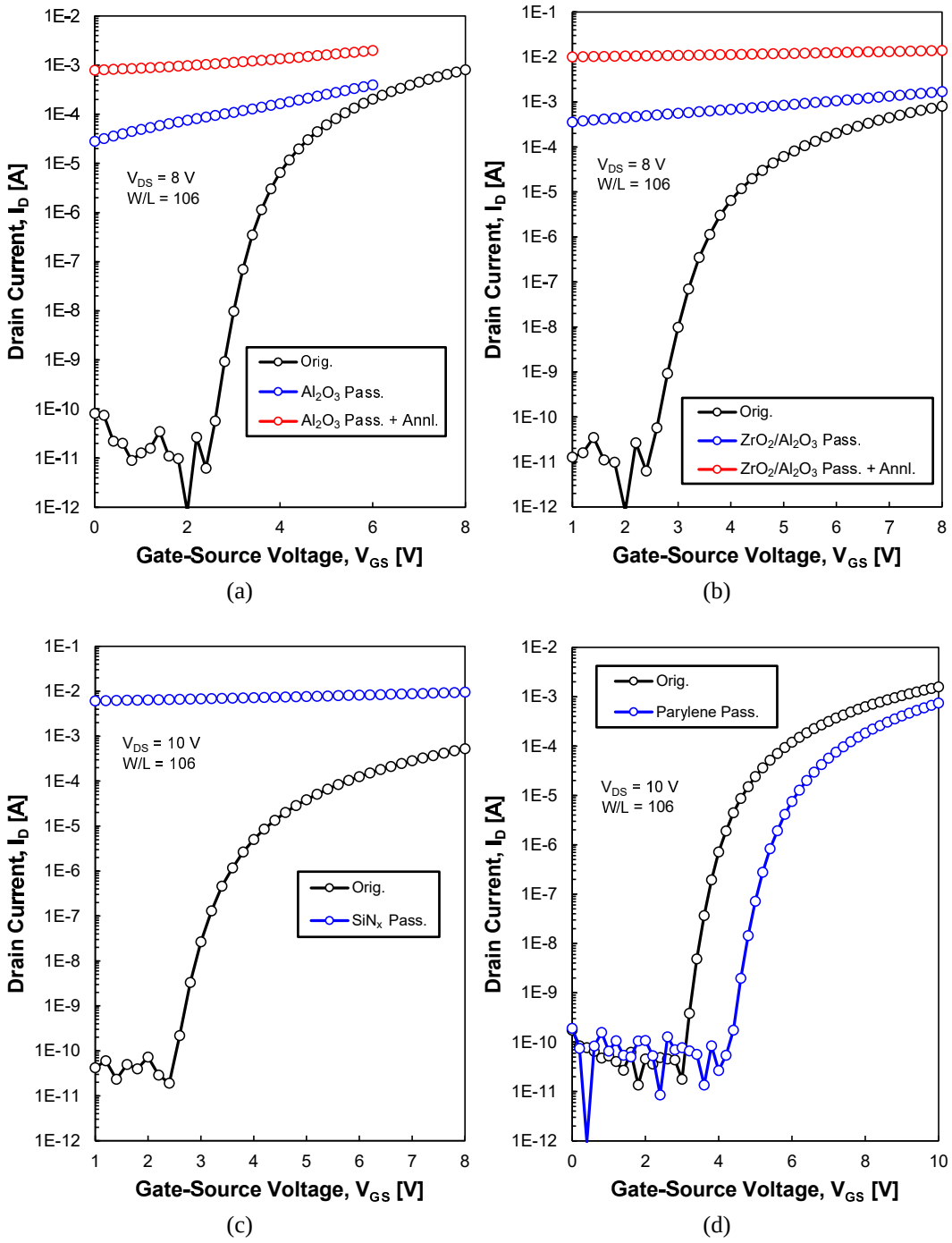


Figure 5.1. Comparison of passivation effects on InGaZnO TFTs: (a) 50 nm ALD Al_2O_3 passivation at T_{dep}=180 °C, (b) 50 nm ALD ZrO_2/Al_2O_3 nanolaminate passivation at T_{dep}= 180 °C, (c) 200 nm PECVD SiN_x passivation at T_{dep}=300 °C, (d) 1 μmParylene passivation at T_{dep} >100 °C.

and V_{TH} (+14.8 V).

Unlike these studies, ALD TiO_x passivation is studied here. The high quality and low

pin-hole density of ALD films makes this technique an ideal method for barrier film formation. Moreover, the ability to deposit the TiO_x with ALD at low temperatures reduces the thermal budget and renders the process compatible with flexible or glass substrates that can be used for both display and wearable electronic applications.

5.2 Fabrication

The samples were fabricated using the third generation TFT layout, with the exception that a 3-inch diameter p++ silicon (Si) wafer was used as the common gate (see Figure 5.2). Thus, a 25 nm thick Al_2O_3 film was first deposited at 250 °C via ALD on the wafer. The Al_2O_3 deposition used trimethylaluminum and water vapor as the aluminum and oxygen source, respectively, yielding a growth rate of 0.9 Å/cycle. A 50 nm thick InGaZnO (In:Ga:Zn = 1:1:5) semiconducting film was then deposited by pulsed laser deposition (PLD) at room temperature and 25 mTorr O_2 using a KrF excimer laser operating at 30 Hz and a 1.8 J/cm^2 energy density. A mesa etch with diluted glacial acetic acid followed to isolate neighboring devices. Subsequently, 25 nm/200 nm thick chrome/gold (Cr/Au) source and drain contacts were formed using electron-beam evaporation and lift-off. The devices consisted of four parallel channels, each with a width (W) of 25 μm and length (L) of 10 μm (see insert in Figure 5.2), thus representing an effective W:L ratio of 10:1. TFTs in this state constitute the bare reference device. Passivation of the devices was accomplished using a two-step process. Initially, the devices were subjected to a N_2O plasma treatment at 50 KHz and 50 W RF power for 2 minutes. In previous work, this has been found to reduce the effect of hydrogen doping during PECVD SiO_2 passivation step [194, 195]. The samples in the form of individual chips were then transferred to an ALD chamber, in which 15 nm thick films of TiO_x were deposited at four temperatures (100 °C, 150 °C, 200 °C and 250 °C). The precursors for TiO_x deposition were water vapor and tetrakis(dimethylamino)titanium (TDMAT). Following passivation, the TFTs were annealed in an O_2 atmosphere at 300 °C for 30 minutes.

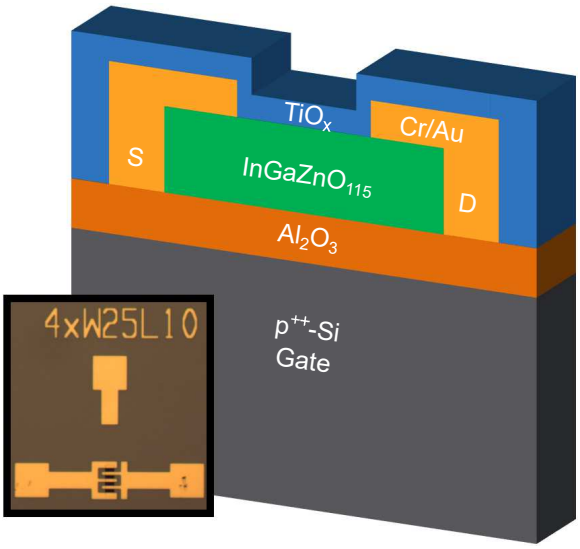
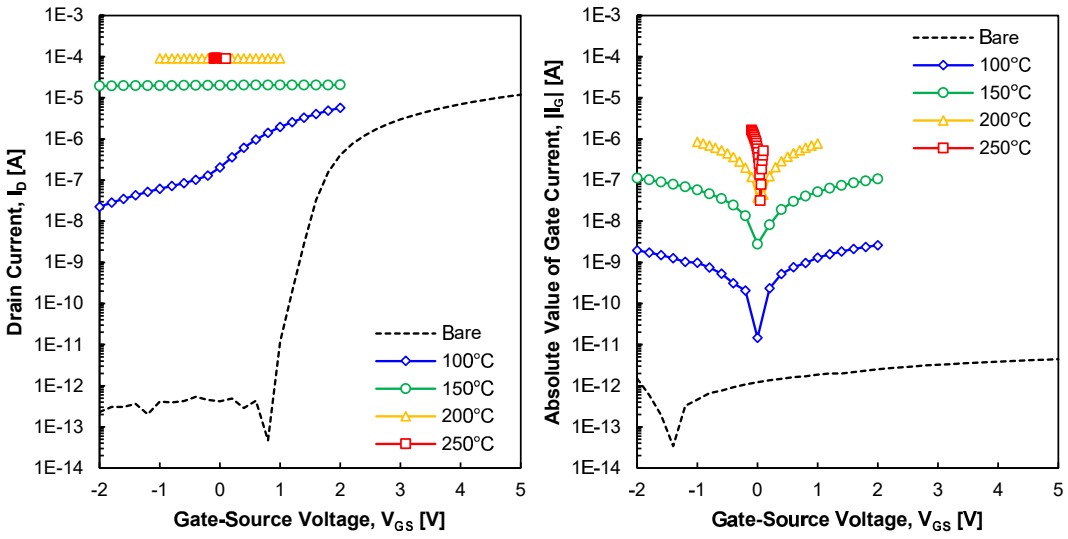


Figure 5.2. Cross-sectional representation and micrograph of the InGaZnO TFTs.

5.3 Results and Discussion

Figure 5.3a presents a comparison of the TFT transfer characteristics in the linear mode of operation (V_{DS} = 0.1V) measured directly after the TiO_x passivation step (prior to O_2 annealing step). The threshold voltage (V_{TH}) is defined as the value of V_{GS} where I_D = 1 nA. The on/off ratio (I_{on}/I_{off}) is calculated by evaluating the ratio of the maximum on-state current to the minimum off-state current. For the bare device, as reported in Section 3.5.2, V_{TH} = 2.2 ± 0.3 V, $\mu_{FE,LIN}$ = 14.1 ± 1.8 $cm^2 V^{-1} s^{-1}$ and S = 167 ± 42.1 mV/dec. It is observed that, in all cases, passivation causes I_{off} to increase, and V_{TH} to shift negative. Moreover, the degree to which these changes occur depends on the deposition temperature. The 100 °C deposition increases I_{off} to 10^{-8} A, while at 250 °C it reaches 10^{-4} A. Figure 5.3b depicts the absolute value of I_G vs. V_{GS} behavior at this stage of the fabrication. The bare device functions well with $|I_G| \sim$ pA, but $|I_G|$ is found to increase significantly with increased passivation deposition temperature.

Each of the samples was then subjected to an O_2 anneal for 30 minutes at 300 °C. After annealing, the gate current (not shown) decreased to less than 100 pA in all of the devices. As shown in Figure 5.4a, the transfer characteristic also improved, with I_{on}/I_{off} increasing to

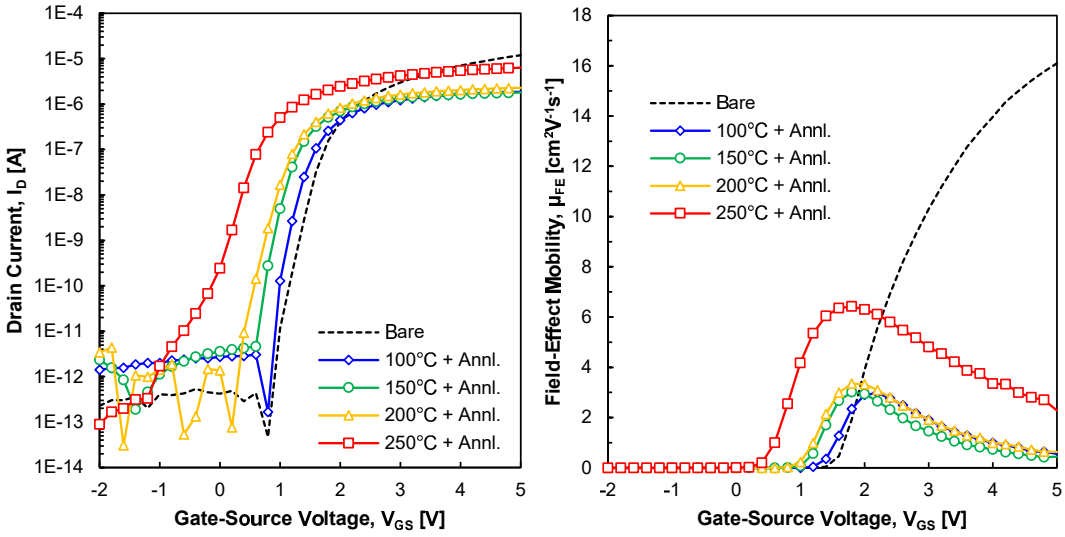


(a) (b)

Figure 5.3. Comparison of (a) transfer characteristics and (b) gate current (I_G) immediately following ALD TiO_x passivation.

10^7 or more. Nonetheless, there remains a performance dependence on the passivation deposition temperature: as before, V_{TH} becomes more negative as the deposition temperature increases. The field-effect mobility is calculated using Equation 2.21. Its V_{GS}-dependent characteristic is plotted in Figure 5.4b.The deposition temperature of the passivation film clearly affects this parameter too. Though the bare device's maximum mobility was 16.5 $cm^2V^{-1}s^{-1}$, the passivated devices all possess significantly reduced values. At 100 °C, $\mu_{FE,max}$ falls to 2.9 $cm^2V^{-1}s^{-1}$ and increases with temperature to 6.5 $cm^2V^{-1}s^{-1}$ at 250 °C.

Table 5.1 summarizes the performance parameters with respect to passivation film deposition temperature. In addition to the abovementioned characteristics, it was found that the sub-threshold swing (S) tends to increase with increasing film deposition temperature. The bare device possesses an excellent S of 140 mV/dec. The device passivated at 100 °C displays a slightly worse value of 185 mV/dec, while the device passivated at 250 °C increases notably to 363 mV/dec. These trends seem to indicate that a higher passivation deposition temperature increases the trap density either in the InGaZnO bulk or the InGaZnO top surface where the TiO_x is introduced. This effect will be explored in more detail below.



(a) (b)

Figure 5.4. Comparison of (a) transfer characteristics and (b) field-effect mobility following the annealing step in O_2 at 300°C after passivation.

Table 5.1. Summary of device characteristics as a function of ALD TiO_x passivation film deposition temperature.

Property	Bare	100 °C	150 °C	200 °C	250 °C
V_{TH} [V]	2.2 ± 0.3	1.1	0.9	0.7	0.2
$\Delta V_{TH,hys}$ [V]	0.7	0.2	<0.1	0.1	<0.1
S [mV/dec]	167 ± 42.1	185	225	170	365
$\mu_{FE,max}$ [$cm^2V^{-1}s^{-1}$]	14.1 ± 1.8	2.9	3	3.4	6.5
I_{on}/I_{off}	2×10^8	2×10^8	1×10^7	9×10^7	5×10^8

Positive bias stress (PBS) tests were conducted on the bare, 100 °C and 250 °C samples to contrast device stability (Figure 5.5). Each device was subjected to a forward bias condition of V_{GS} = 5V and V_{DS} = 0.1V for 3600 sec (1 hour). The bare device experienced a +1.1V shift in V_{TH}. In comparison, V_{TH} of the 100 °C passivated device decreased by 0.2 V. Lastly, the 250 °C passivated device was observed to be the most stable of the devices, showing a nearly negligible 0.05 V positive threshold voltage shift. These results support previous reports [196] showing that the device stability is not solely dependent on the bottom dielectric (Al_2O_3)-InGaZnO interface, but is also highly dependent on the electric field-induced adsorption of oxygen and desorption of water that the TiO_x successfully suppresses. S was also affected differently following stress depending on the temperature of

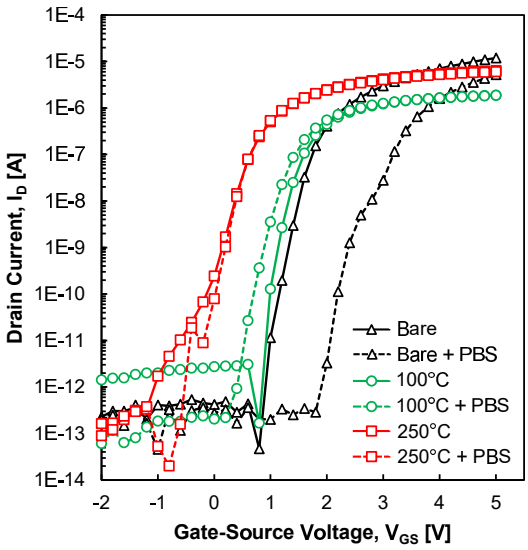


Figure 5.5. Positive bias stress (PBS) results for the bare, 100 °C and 250 °C ALD TiO_x passivated devices.

the passivation deposition. S in the bare device increased from 140 mV/dec to 216 mV/dec, in the 100 °C device it only increased from 185 mV/dec to 190 mV/dec, while in the 250 °C device it improved from 363 mV/dec to 295 mV/dec.

To better understand the above results, time-of-flight secondary ion mass spectroscopy (TOF-SIMS) was carried out on select devices. In past studies, TOF-SIMS has been used to show that high temperature ICP-CVD SiO_x passivation can cause diffusion of In, Ga and Zn into the SiO_x passivation layer, in turn causing reductions in μ_{FE} and increases to S [197]. Furthermore, it has been reported that differences in the type of precursor (O_2 vs. H_2O vapor) used for plasma-enhanced vs. thermal ALD Al_2O_3 passivation, respectively, can influence hydrogen doping, which subsequently determines V_{TH} shift [198]. In Figure 5.6, O_2 is used to sputter through the TiO_x-InGaZnO layers of the TFT and obtain a cross-sectional understanding of the chemical composition. The normalized concentrations of Ti^+, Ga^+, $113In^+$, $68Zn^+$ and H^+ are all plotted with respect to the total number of counted elements. Isotopes of In and Zn are tracked in stead of the base element because of their more distinct masses, which reduces the risk of false positives. It is observed that in both samples, where TiO_x has been deposited at 100 °C and 250 °C, respectively, there does

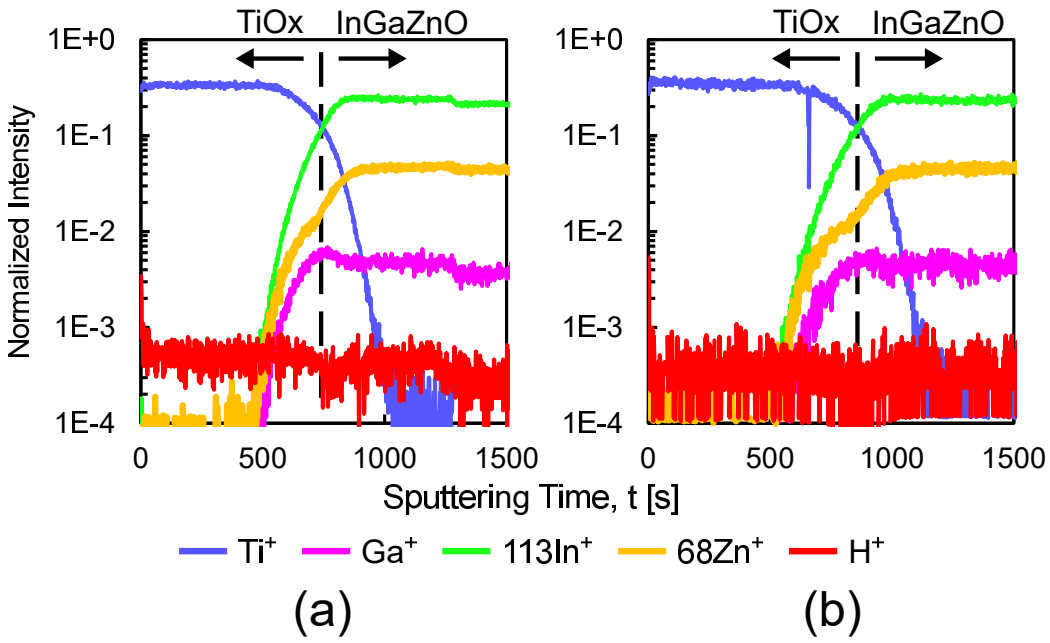
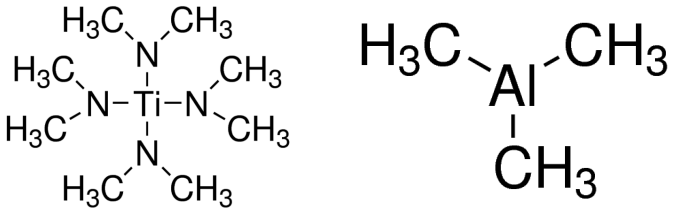


Figure 5.6. TOF-SIMS depth profile for the TiO_x passivated samples at (a) 100 °C and (b) 250 °C.

not appear to be a different in interdiffusion of these elements. Moreover, it seems that the presence of hydrogen is the same in both cases. Hence, TOF-SIMS analysis on these samples indicates that tere are negligible differences in interdiffusion or hydrogen doping due to temperature effects.

As an alternative to the above explanations from the literature, the effect of oxygen gettering by the TiO_x film is considered. It is well understood that oxygen vacancies act as electron donors in InGaZnO films. It has also been found that Ga plays an important role as an oxygen getter in this system, improving both the mobility and V_{TH} stability over InZnO films [199]. Yen et al. recently reported that TiO_x competes with Ga for oxygen [200]. They used e-beam evaporation to deposit TiO_2 on both InGaZnO (1:1:1) and InZnO (1:1) TFTs prior to S/D contact formation. Both the InGaZnO and InZnO TFTs experienced negative shifts in V_{TH}, which was attributed to the creation of oxygen vacancies due to gettering. It was additionally seen that whereas S improved for the InGaZnO TFTs, it deteriorated in the InZnO TFTs. This difference was explained by the absence of Ga in InZnO, and further supports the theory that Ga plays a stabilizing role in InGaZnO.



(a) (b)

Figure 5.7. Molecular representation of metal-organic precursors used for ALD of: (a) TiO_x - tetrakis(dimethylamido)titanium (TDMAT), (b) Al_2O_3 - trimethylaluminum (TMA).

Table 5.2. Bond energies for ALD precursors at T = 298 K [202].

Material	BE_{M-O} [kJ mol^{-1}]	BE_{M-L} [kJ mol^{-1}]	ΔBE [kJ mol^{-1}]
TiO_x	662 Ti-O	464 Ti-N	198
Al_2O_3	512 Al-O	255 Al-C	257

The effect of gettering can be better understood through a closer examination of the competing bond energies during passivation [201]. As explained in Section 3.3.3, ALD works by exposing the target substrate to a sequential order of metal-organic gas-phase precursors. The tendency for the precursor to extract oxygen from the InGaZnO film can be expressed as the difference between the metal-oxygen (BE_{M-O}) and metal-ligand (BE_{M-L}) bond energies:

$$\Delta BE = BE_{M-O} - BE_{M-L} \tag{5.1}$$

For example, the metal-organic precursors used for ALD TiO_x and Al_2O_3 are shown in Figure 5.7. In the case of TiO_x deposition, where tetrakis(dimethylamido)titanium (TDMAT) is used, Ti must break free from N. However, Al is bonded to C in trimethylaluminum (TMA) used for and Al_2O_3. The resulting bond energies are summarized in Table 5.2, where it can be concluded that Al is more likely to getter O_2, which could explain the highly conductive nature of the Al_2O_3 passivated TFTs seen in Figure 5.1a.

Our measurements show that the TiO_x passivation induces a temperature-dependent reduction in V_{TH} that could be also be linked to an increase in oxygen vacancies due to O_2 gettering by TiO_x. Therefore, we propose that the effect of oxygen gettering is influenced by the deposition temperature, with higher deposition temperatures inducing stronger gettering that increases the number of oxygen vacancies, and results in a reduced threshold voltage. The increase in S with passivation film deposition temperature is likewise explained by the generation of traps from this phenomenon. Moreover, our results further elucidate the role of the InGaZnO composition in determining the compatibility of passivation strategies. Whereas Ye et al. used a 1:1:1 target, our work used a 1:1:5 composition that is more akin to Ga-absent InZnO. Therefore, care must be taken in choosing the composition of InGaZnO, as well as its thin film deposition conditions, when selecting a passivation material and deposition process.

5.4 Conclusion

This work reveals that the deposition temperature of TiO_x for passivation of $InGaZnO_{115}$ TFTs plays a critical role in determining the performance of the device. As the deposition temperature increases, V_{TH} shifts downward and S increases. All of the TiO_x passivated devices were found to have reduced $\mu_{FE,max}$ compared to the bare reference, while higher deposition temperatures offered the highest mobility. Moreover, positive bias stress induced threshold voltage shift was reduced following passivation. Overall, it has been found that low temperature (i.e., 100 °C) deposition of the passivation film best preserves the device characteristics, except for mobility. For application of chemical sensors, high mobility has not been identified as a key device attribute, and therefore the low-temperature ALD TiO_x passivated InGaZnO TFTs can be investigated for liquid-phase sensing applications.

It is proposed that these results are explained by the formation of oxygen vacancies in the InGaZnO film due to oxygen gettering, and point to the material composition's importance in determining a TFT's sensitivity to passivation material and process conditions.

In the future, further experimentation is required to confirm the gettering effect. The use of TOF-SIMS did not allow tracking of O_2 content since O_2 was used as the sputtering element. An alternative chemical analysis tool, such as XPS, could be used instead, and would provide additional information regarding the binding energies. Specifically, the oxygen content of TiO_x-only samples could be compared to samples with TiO_x on InGaZnO to confirm whether the TiO_x on InGaZnO incorporates more oxygen due to gettering.

CHAPTER 6

DUAL-GATE InGaZnO THIN FILM TRANSISTORS FABRICATED AT LOW TEMPERATURE FOR HIGH-SENSITIVITY pH SENSING

Building on the successful low-temperature passivation of InGaZnO TFTs using ALD TiO_x that was presented in Chapter 5, dual-gate InGaZnO TFTs with high-ϵ_r dielectrics are investigated for high-sensitivity pH sensing. Unlike previous works that have high temperature thermal oxide growth to realize these devices, this work employs entirely low temperature fabrication methods, rendering them compatible with low-cost and flexible substrates used in future wearable electronics. The impact on sensitivity when using either PECVD SiO_2/SiN_x or ALD TiO_x passivation films, which also serve as the liquid sensing gate, is compared. It is found that ALD TiO_x offers a sensitivity of 76 mV/pH, which is beyond the Nernst limit found in traditional ISFET sensors. Moreover, after microfluidic packaging is implemented, it is found that reliable sensor performance in liquid can be achieved over the course of several hours.

6.1 Prior Art

The original FET-based pH sensor is the ion sensitive field effect transistor (ISFET) that was first proposed by Bergveld (Figure 6.1a) [77, 78]. This device is derived from the traditional Si-based CMOS nFET, except that the gate metal contact is removed and replaced by the liquid analyte of interest, as well as a reference electrode through which V_{GS} is applied. The reference electrode is typically silver/silver chloride (Ag/AgCl) or, in some cases, a bare platinum (Pt) or silver (Ag) wire. Detection of the fluid's pH level is achieved by monitoring shifts in the ISFET's V_{TH}, which arise from the modulation of charge in the ISFET's channel depending on the charge that is accumulated at the liquid-dielectric interface. Thus, it can be considered that the function of the original gate contact is substituted by the presence of ions in the liquid. When an acidic liquid (i.e., pH < 7) is used, positively

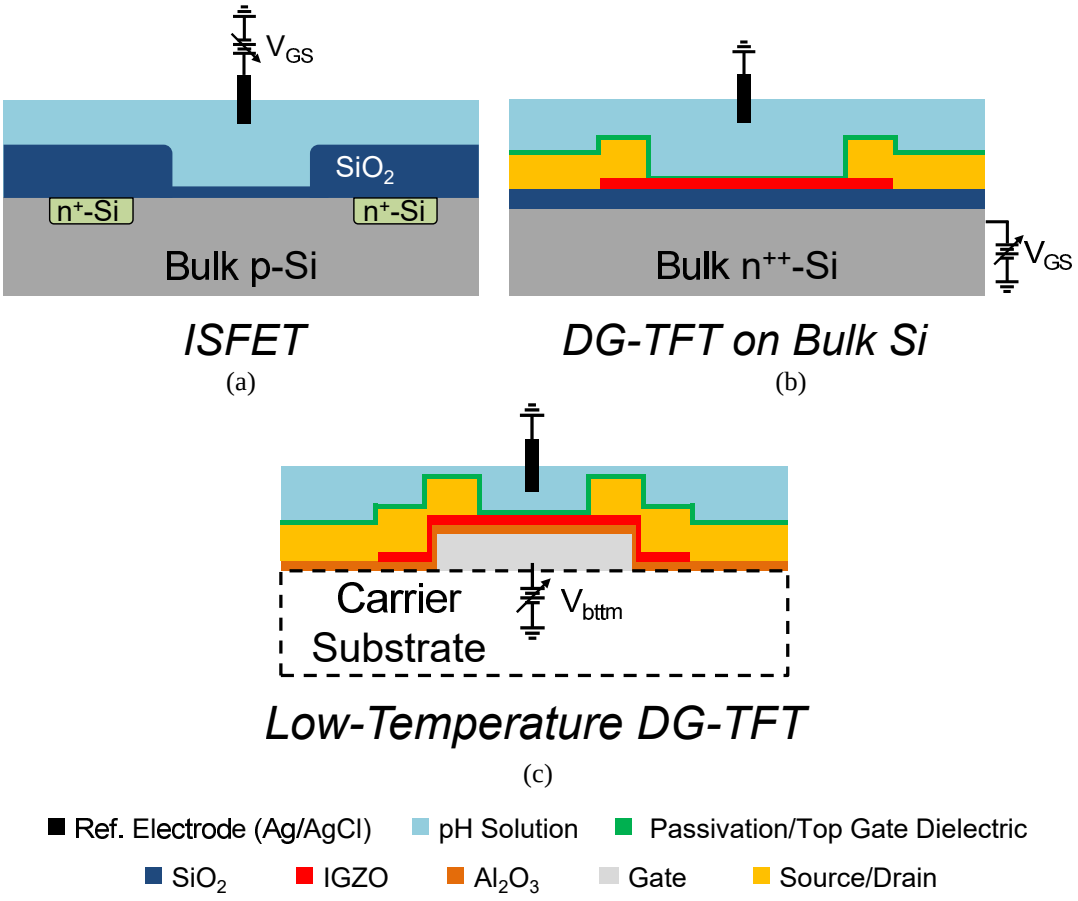


Figure 6.1. Evolution of FET-based pH sensors: (a) the traditional ion sensitive field-effect transistor (ISFET) uses the standard Si-CMOS nFET and is limited in sensitivity by the Nernst Limit (i.e., ~59 mV/pH), (b) double-gated thin film transistor (DG-TFT) on silicon substrate with thick, thermal oxide (SiO_2) bottom gate dielectric and sensitivity beyond the Nernst Limit, (c) low-temperature fabricated DG-TFT that is compatible with both Si and alternative substrate materials while providing sensitivity beyond the Nernst Limit.

charged H^+ ions effectively apply a positive gate bias that reduces V_{TH}. Alternatively, when a basic solution (i.e., pH > 7) is used, OH^- ions shift V_{TH} upward. Under ideal conditions, the Nernst Limit, which describes the maximum shift in V_{TH} per unit pH change, of 59 mV/pH defines the upper boundary of the ISFET's sensitivity. To reach the Nernst Limit, SiO_2 is often replaced by other high ϵ_r dielectrics, such as TaO_x or Al_2O_3. The fact that these devices can be produced using CMOS-compatible processes, with some additional post-processing, has led to high levels of system integration and, in some cases, advanced biological sensing applications [203, 204]. Highly reliable ISFET-like sensors have also been demonstrated with other TFT technologies, such as OTFTs [205].

The extended gate (EG) FET [206] is a variant of the ISFET, which seeks to increase reliability by separating the sensing area from the FET device. By isolating the FET from the liquid, the risk of hydrolysis is minimized. This configuration has been explored for InGaZnO using low temperature deposition processes, both on flexible [207,208] and glass [209] substrates. However, the maximum sensitivity is still defined by the Nernst Limit, with sensitivities in the range of 40-50 mV/pH having been reported so far.

To overcome the Nernst Limit, a novel approach to pH sensing involving double-gated (DG) TFTs, as shown in Figure 6.1b has been developed. Organic [79], ZnO [80], and InGaZnO DG-TFTs [81,82] have all been investigated. Hybrid DG-TFT/EGFET InGaZnO have also been reported [81, 210]. Though sensitivities as high as 2.25 V/pH have been shown, all of these investigations share a common shortcoming: they rely on the use of a thick, thermally grown SiO_2 bottom gate dielectric. This means that neither transparent glass, nor flexible plastics can be used as substrates. In addition to these works, it should also be noted that a recent study claimed "Super-Nernstian" pH sensitivity using an unpassivated InGaZnO DG-TFT [211]. Since it is well known that even highly diluted acidic solutions can be used to etch InGaZnO, the direct exposure of the InGaZnO film to pH solutions raises concerns over long term reliability.

Hence, the aim of the work in this chapter is to develop a reliable InGaZnO DG-TFT using low-temperature fabrication steps that exhibits sensitivity beyond the Nernst Limit (see Figure 6.1c). This is accomplished through the use of high-ϵ_r dielectrics deposited using ALD below 180 °C. For comparison with the top-gate ALD TiO_x dielectric, traditional PECVD SiO_2/SiN_x is also studied. Moreover, the development of a microfluidic packaging for this sensor enables reliable device operation.

6.2 Dual-Gate TFT Sensing Theory

In order to understand why the DG-TFT configuration gives rise to a "Super-Nernstian" pH sensitivity, a closer look at the operation of the device is necessary. The transfer function for

a DG-TFT from ΔpH to ΔV_{TH} can be derived from the single-gated field-effect transistor's drain current (I_D) operated in the linear regime, and assuming a small value of V_{DS} in Equation 2.11:

$$I_D = \frac{WC_i'\mu}{L}(V_{GS} - V_{TH})V_{DS} \tag{6.1}$$

By analogy, I_D for the DG-TFT can be expressed as two parallel current sources [8]:

$$I_D = \frac{W\mu}{L}\left[C_{i,top}'(V_{top} - V_{TH,top}) + C_{i,bttm}'(V_{bttm} - V_{TH,bttm})\right]V_{DS} \tag{6.2}$$

where the top and bottom gate-source applied voltages and threshold voltages are now described by V_{top}, $V_{TH,top}$, V_{bttm}, and $V_{T,bttm}$, respectively.

For sensing applications, V_{top} is held constant by tying it to the grounded source terminal ($V_{top} = 0$). In this configuration, Equation 6.2 can be re-arranged as

$$I_D = \frac{W\mu}{L}C_{i,bttm}'(V_{bttm} - V_{TH,eff})V_{DS} \tag{6.3}$$

where the effective threshold voltage, $V_{TH,eff}$, is

$$V_{TH,eff} = V_{TH,bttm} - \frac{C_{i,top}'}{C_{i,bttm}'}V_{TH,top} \tag{6.4}$$

Since only the top gate is exposed to the analyte fluid, any change in $V_{TH,eff}$ arises from changes to $V_{TH,top}$. Thus,

$$\Delta V_{TH,eff} = -\frac{C_{i,top}'}{C_{i,bttm}'}\Delta V_{TH,top} \sim -\frac{C_{i,top}'}{C_{i,bttm}'}\Delta\Psi_0 \tag{6.5}$$

where Ψ_0 represents the top gate-electrolyte interface potential. Bergveld's analysis showed [1]

$$\Delta\Psi_0 = \left(-2.3\frac{kT}{q}\alpha\right)\Delta pH \tag{6.6}$$

where k is the Boltzman constant, T is the temperature, q is the charge of a single electron, α is a constant which depends on the quality of the dielectric-analyte interface and ΔpH is the change in pH. For an ideal dielectric (α=1) and at room temperature (T = 300K), $\Delta\Psi/\Delta pH$ -59 mV/pH; this is what is referred to as the Nernst sensitivity limit. From Equations 6.5 and 6.6, therefore, it can be seen that with careful selection of the top and bottom dielectric materials and thicknesses, the DG-TFT's sensitivity can be greater than the Nernst Limit.

6.3 Achieving "Super-Nernstian" Sensitivity

This section discusses the development of low-temperature InGaZnO DG-TFTs with sensitivities beyond the Nernst Limit.

6.3.1 Sample Preparation

The InGaZnO TFTs used in this part are fabricated on Si wafers using the second generation design described in Chapter 3. Room-temperature PLD InGaZnO (1:1:1) deposited at AFRL (unlike the 1:1:5 type studied in Chapter 5) is deposited on top of a 50 nm thick ALD Al_2O_3 bottom gate dielectric. Post-fabrication annealing at 300 °C for 30 min in air was also employed. It should be underlined that the Si wafer serves only the role of a carrier substrate, and therefore the low-temperature process of fabricating these TFTs can be directly transferred to other temperature-sensitive substrates in the future, as has already been demonstrated in Section 3.5.1.1.

In this section, the suitability of two passivation films for this application are compared, both in terms of how they affect the current-voltage (I-V) characteristics of the TFT, as well as their impact on pH sensing. The first passivation scheme, that also serves as a control, consists of a dual layer of 150 nm SiO_2 and 50 nm SiN_x, both deposited via PECVD at 300 °C. A N_2O plasma treatment step is also used before depositing these materials. The second passivation layer that was investigated was a 10 nm thick ALD TiO_x film deposited at 100 °C. The use of ALD is advantageous for this application since it has excellent step coverage,

and is therefore capable of isolating the source/drain fingers from the liquid despite its small thickness. As mentioned previously, this is important in order to avoid hydrolysis and subsequent leakage currents (tests done using a bare TFT in liquid resulted in rapid device deterioration). TiO_x was specifically chosen due to its high-ϵ_r nature (typically in the range of 26-100) that would increase $C_{i,top}$ and therefore improve sensitivity.

In this iteration, a simple PDMS reservoir was used to confine the pH solutions around the TFTs, and away from the outer probe pads shown in Figure 3.3a. A Ag/AgCl reference electrode was derived by soaking a 99.9% pure Ag silver wire in bleach for 20 minutes at room temperature. This electrode was then connected to the TFT's source terminal to ensure a common ground across the circuit.

6.3.2 I-V Characteristics Comparison

Figure 6.2 shows a comparison of the transfer characteristic (V_{GS} vs. I_D) for a N_2O-SiO_2-SiN_x passivated TFT before and after passivation. Voltage sweeps are performed in both the positive and negative directions in order to observe hysteresis ($\Delta V_{TH,HYS}$). The device is biased in saturation with V_{DS} = 5 V. The bare device has an average V_{TH} of 2.8 V, a ΔV_{TH} of 278 mV, an on/off ratio of 10^7, sub-threshold swing (S) = 310 mV/dec and saturation field-effect mobility ($\mu_{FE,SAT}$) = 4 $cm^2V^{-1}s^{-1}$. By comparison, the passivated device has an average V_{TH} of 0.31 V, a $\Delta V_{TH,HYS}$ of 42 mV, an on/off ratio of 10^{10}, S = 290 mV/dec and $\mu_{FE,SAT}$ = 5.6 $cm^2V^{-1}s^{-1}$. In all aspects, the device performance has improved as a result of passivation. This is thought to be due to protection of the InGaZnO back surface from moisture and other environmental effects that cause electron scattering, which reduce mobility as well as mobile charges, which increase hysteresis. However, V_{TH} experiences a significant -2.5 V shift after passivation.

The effect of ALD TiO_x passivation on the TFT is shown in Figure 6.3. The device is again biased in saturation with V_{DS} = 5 V. The bare device has an average V_{TH} of 1.56V, a $\Delta V_{TH,HYS}$ of 22 mV, an on/off ratio of 10^{12}, S = 335 mV/dec and $\mu_{FE,SAT}$ = 3 $cm^2V^{-1}s^{-1}$. The passivated device has an average V_{TH} of 1.58 V, a $\Delta V_{TH,HYS}$ of 27 mV, an on/off ratio

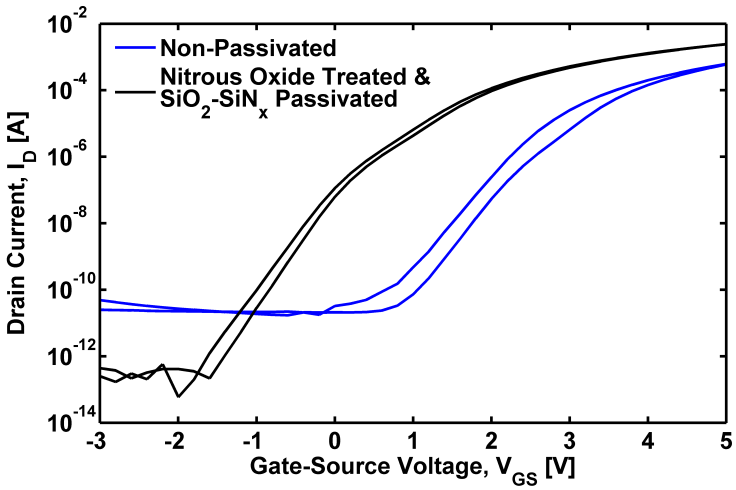


Figure 6.2. I_D-V_{GS} transfer characteristics of TFT with 5 μm channel length before (blue curves) and after (black curves) N_2O treatment and SiO_2/SiN_x passivation (V_{DS}=5 V). The SiO_2 and SiN_x films were deposited via PECVD at 300 ºC and the device was subsequently annealed at 300 ºC for 60 minutes in atmosphere.

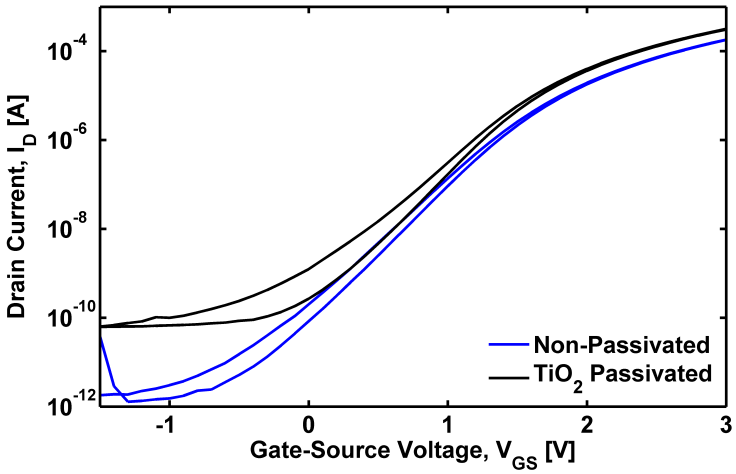


Figure 6.3. I_D-V_{GS} transfer characteristics of TFT with 5μm channel length before (blue) and after (black) passivation with TiO_x (V_{DS}= 5 V). The TiO_x was deposited via ALD at 100 ºC and the device was subsequently annealed at 300 ºC for 60 minutes.

of 10^7, S = 350 mV/dec and $\mu_{FE,SAT}$ = 5.6 $cm^2V^{-1}s^{-1}$. In this case, the device performance, including V_{TH}, remains largely unchanged. The main difference that is observed is an increase in off current, which leads to a decrease in the on/off ratio. One explanation behind this is that there is leakage through the TiO_x passivation layer due to electric-field induced breakdown between the source and gate metal lines on the top surface.

6.3.3 pH Sensing

Devices of each kind were then used for pH testing. For each buffer solution, five consecutive transfer sweeps were obtained. The devices were operated in the linear region (V_{DS} = 0.5 V), in order to avoid faradaic leakage currents that arise due to hydrolysis of the liquid analyte. Figure 6.4 shows the result for one such measurement conducted on a TiO_x-passivated TFT using a test sequence of pH = 6, 8, 6, 8. It is observed that the devices operated in a stable fashion within this aqueous environment. Moreover, the change in pH results in a repeatable horizontal shift in the curves that is explained by a change in the top-gate V_{TH}; the direction of the shift agrees with the theory outlined above.

In Figure 6.5, a comparison of sensing performance between the N_2O-SiO_2-SiN_x and TiO_x passivated dies is shown for a test sequence of pH = 5, 9, 5. To better quantify the shift in V_{TH}, the data is converted to show the change in V_{GS} for a fixed reference current (I_D = 3.5 μA). The N_2O-SiO_2-SiN_x passivated device shows no change in V_{TH}. This is expected due to the use of a thick, dual-layer passivation layer that forms two series-connected, low-ϵ_r capacitors with a low total capacitance ($C_{g,top}$). Thus, the DG-TFT is effectively isolated

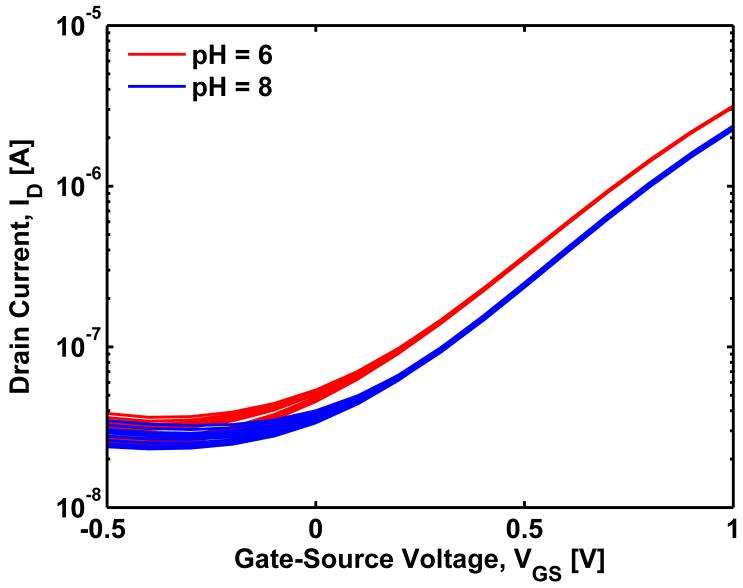


Figure 6.4. I_D-V_{GS} transfer characteristics of a TiO_x-passivated TFT (L = 5 μm) with V_{DS} = 0.5 V exposed to buffer solutions with pH = 6 and 8. The horizontal shifts in the curves demonstrate how V_{TH} is affected by the change in pH.

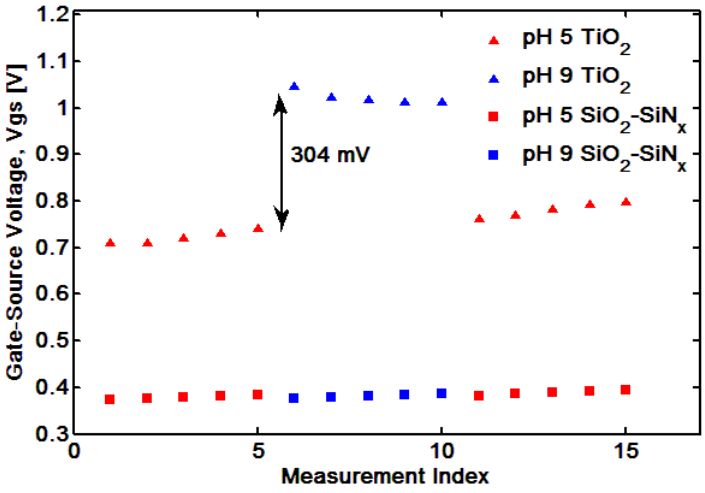


Figure 6.5. Comparison of pH sensing performance between the SiO_2/SiN_x- and TiO_x-passivated TFTs as a function of gate-source voltage (V_{GS}) shift (V_{DS} = 0.5 V). The former is insensitive to changes in pH, while the TiO_x-passivated TFT shows sensitivity beyond the Nernst limit.

from the analyte above. In contrast, the TiO_x passivated sensor sees a V_{GS} increase of 304 mV when the pH changes from 5 to 9. This corresponds to a sensitivity of 76 mV/pH, which is greater than the Nernst sensitivity limit and validates the operation of the DG-TFT sensor. It should be noted that the sensitivity achieved here is lower than what was expected (i.e., >200 mV/pH). One potential explanation for this is that, with reference to equation 6.6, the ALD TiO_x as currently deposited is non-optimal (i.e., $\alpha < 1$). Further investigation is required to verify this. One possibility for doing this would be to use a single-gate, extended gate configuration, where ALD TiO_x is used as the sensing film, as has been done when to study other novel sensing materials , such as carbon nanotubes [212]. In this way, the ALD deposition recipe can be optimized with respect to pH sensitivity.

6.4 Achieving Reliable Performance with Microfluidic Packaging

The above devices successfully achieved sensitivities beyond the Nernst Limit. However, they suffered from a lack of stability, as well as the inability to operate in liquid for prolonged period of time. After a few hours of exposure to liquid, the devices would degrade

and FET-like performance was no longer observable. This section discusses the development of an improved microfluidic package that offers the ability to operate the InGaZnO DG-TFT sensors for significantly longer periods.

6.4.1 Sample Preparation

Section 3.2.3 described the device and die layouts used in Generation 3. As mentioned there, in addition to the 4-mask process required to fabricate the InGaZnO TFTs, two additional masks were designed for the microfluidic structures. The first introduces a 6 μm thick SU-8 film (SU8-3005) above the top dielectric layer that is patterned such that only the TiO_x sensing regions are exposed to the liquid. The second mask permits the fabrication of a Si-based master mold for PDMS casting. The PDMS can then be bonded to the SU-8 to form microfluidic channels across the die for liquid analyte delivery.

Figure 6.6a shows a picture of the die after the first packaging step where the PDMS microfluidic structure has been attached on top of the device chip. The large circles on the die defined by the S/D metal layer are used to visually align the PDMS to the on-die features. Two tubes have been inserted into the inlet and outlet port of the PDMS. It was initially intended to semi-permanently bond the PDMS to the SU-8 using a N_2-plasma based bonding treatment [213]. Though successful implementation of this approach was achieved using test samples, it could not be replicated on the device dies. It is thought that this is because the amino-activated surface of the PDMS can only bond to SU8 when it has not fully cross-linked, and therefore residual epoxy groups are available. These could not be preserved on the active die because of the extra baking steps necessary during dicing preparation. As a result, an alternative strategy was adopted that introduces a clamping structure to ensure a good seal between the SU8 and PDMS. The parts for the clamping structure, shown in Figure 6.6b are made from poly(methyl methacrylate), or PMMA. These were cut out using a CO_2 laser. As shown in Figure 6.6c and 6.6d, the final system consists of the TFT die and PDMS microfluidics sandwiched between the PMMA components.

The pH measurements with this package were taken within a dark box and on top of a

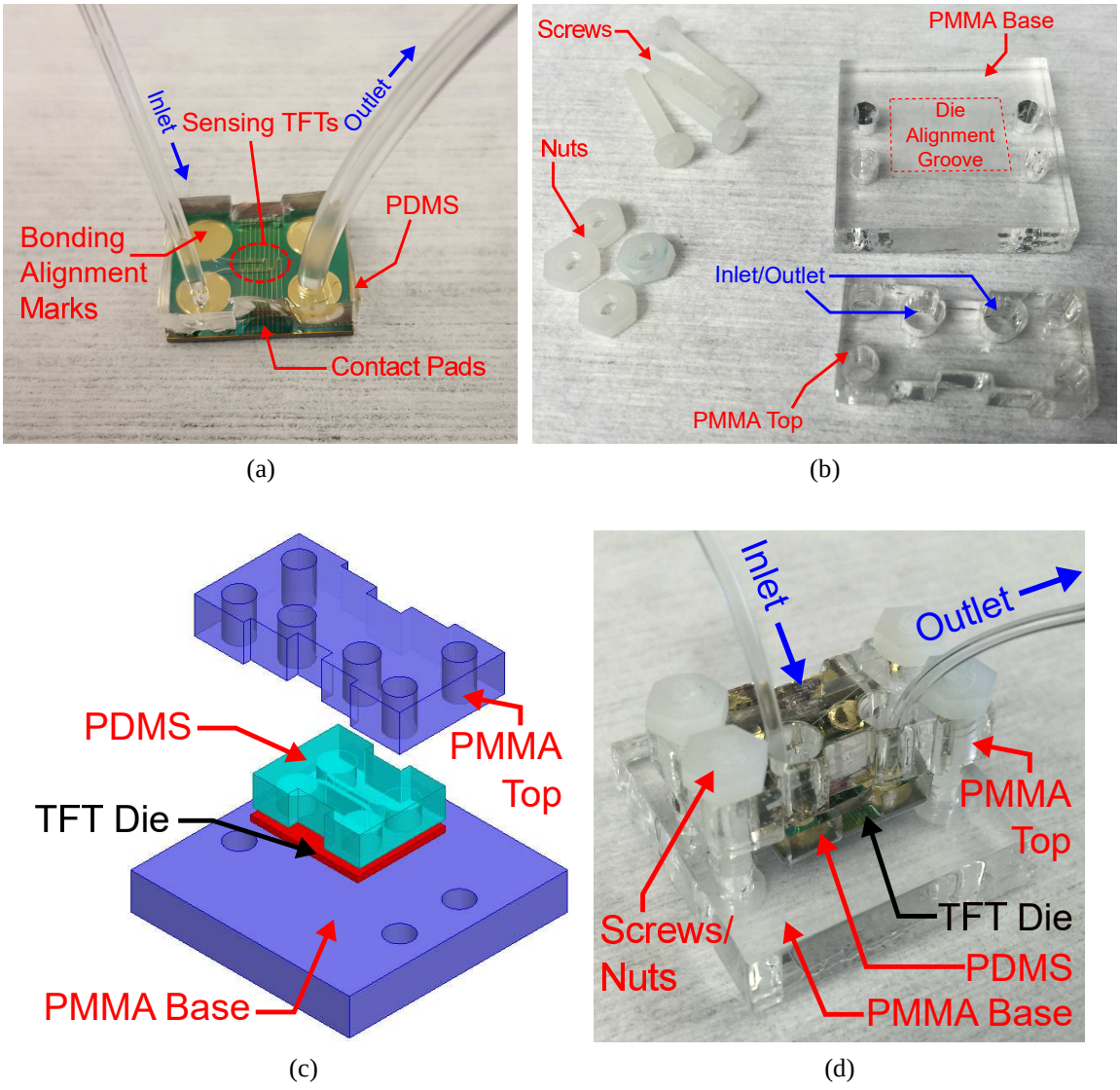
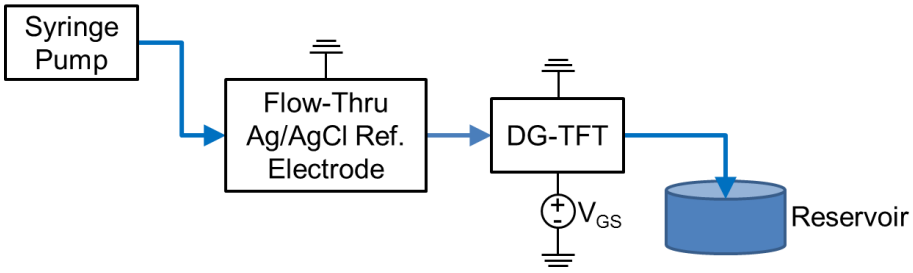
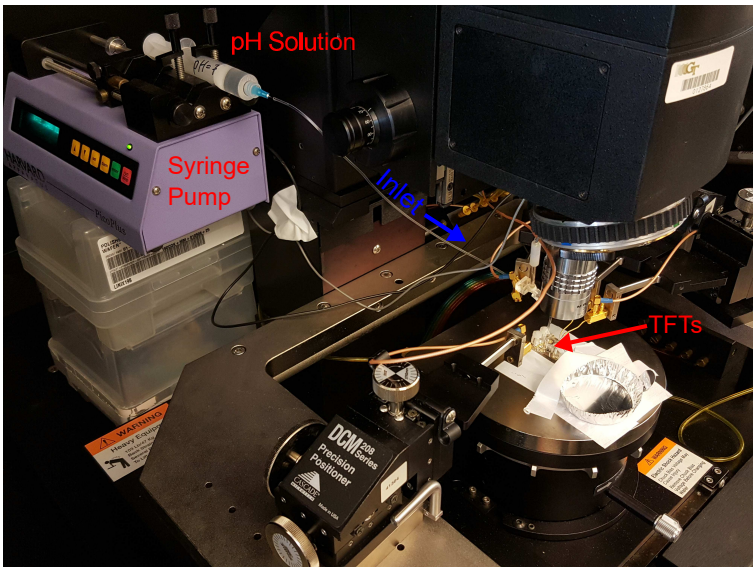


Figure 6.6. Summary of microfluidic packaging: (a) Photograph of the PDMS microfluidic cell on top of SU-8 coated InGaZnO DG-TFT with ALD TiO_x passivation/sensing film, (b) collection of CO_2 laser-cut PMMA parts used to create clamp, (c) exploded model view of the entire microfluidic cell (d) photograph of fully packaged TFT within the microfluidic cell.

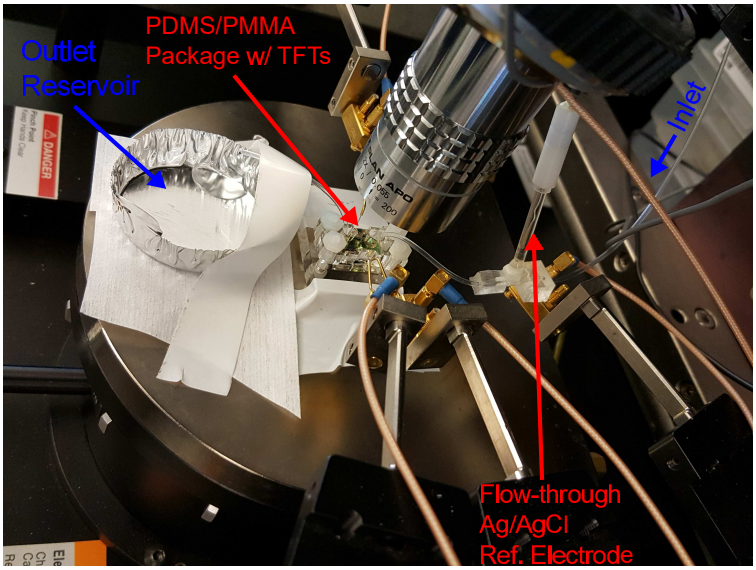
probe station (Figure 6.7). A motorized syringe pump was used to controllably flow the pH solutions into the microfluidic cell where the TFTs are located (Figure 6.7b). In stead of using a simple wire for the reference electrode, this setup permitted the use of a commercial flow-through Ag/AgCl electrode within a potassium chloride (KCl) bath (Figure 6.7c). This further improved the repeatability of the measurements.



(a)



(b)



(c)

Figure 6.7. (a) Overview of pH sensing test setup, (b) photograph of the measurement setup within a dark box and probe station, (c) close-up photograph of pH sensing measurement setup.

6.4.2 Evaluation of Liquid-Phase Operational Stability

The operational stability in liquid and long-term reliability were evaluated using a PLD InGaZnO (1:1:5) TFT with W/L = 2. InGaZnO (1:1:5) was chosen over (1:1:1) for this test because the former has a significantly faster etch rate in acid. For example, when using glacial acetic acid that has been diluted in DI water 1:150, a 50 nm thick InGaZnO (1:1:5) film is completely etched within 10 min. The same etchant requires ≥35 minutes to etch through InGaZnO (1:1:1). Thus, the goal was to evaluate whether a passivated InGaZnO (1:1:5) TFT could operate in liquid over an extended length of time, in turn affirming that these devices can be used in the field.

Figure 6.8a shows the I-V curves that were periodically collected for the liquid-exposed device over a 24-hour period, where a pH = 5 is used. In between these measurements, the devices were unbiased. The TFT continues to operate throughout the entire test, with very little V_{TH} shift observed. As time passes, the OFF current decreases, thus improving the on/off ratio. The sensing baseline drift was monitored by observing two reference current points. At $I_{REF} = 9 \times 10^{-7}$A, the average V_{TH} drift is ≤2 mV/hour, as shown in Figure 6.8b. Additionally, Figure 6.8c demonstrates that for $I_{REF} = 1 \times 10^{-8}$A, the average V_{TH} drift is ≤1 mV/hour. It is of interest that the drift in between the sets of measurement is smaller than the drift observed within each measurement set. This indicates that bias stress effects have a larger effect on stability than the operation in liquid itself.

6.5 Conclusion

Traditional silicon-based ISFETs have a maximum sensitivity of 59 mV/pH that poses limitations on the applicability of these sensors for high-fidelity biomolecule detection. DG-TFTs have been found to offer sensitivity beyond the Nernst Limit, but implementations so far have relied on thermal oxide growth to minimize the bottom gate capacitance. However, the high temperatures required for this step rule out the use of flexible or cost-effective substrates, such as glass or plastic. In this work, InGaZnO-based DG-TFTs with

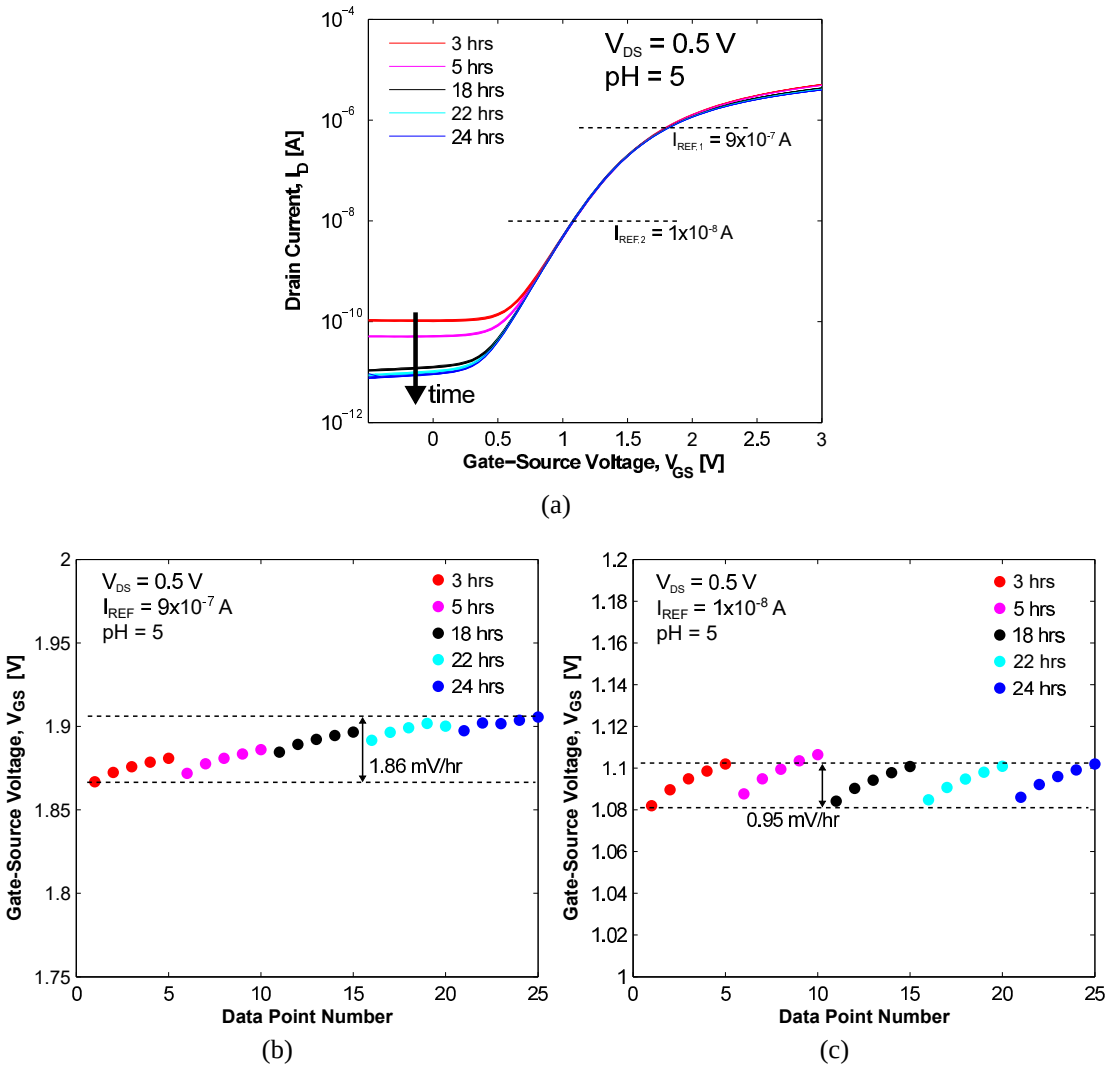


Figure 6.8. 24-hour evaluation of performance and stability in liquid environment (pH = 5): (a) $V_{GS}-I_D$ characteristic, (b) transient response for $I_{REF} = 9 \times 10^{-7}$A, (c) transient response for $I_{REF} = 1 \times 10^{-8}$A.

low-temperature ALD dielectrics have been used to provide "Super-Nernstian" sensitivity while remaining thermally compliant with the aforementioned alternative substrates. A sensitivity of 76 mV/pH has been demonstrated, and is expected to improve with further investigation of thin film material selection and optimization of growth conditions. Crucially, the development of microfludic packaging for these devices has resulted in highly stable and reliable operation in in liquid. When exposed to a pH = 5 solution over the course of 24 hours, the rate of change of V_{TH} was observed to be as low as ≤1 mV/hour.

CHAPTER 7

INTEGRATED InGaZnO PHOTOTRANSISTOR/TPN-Cl_2 Zn ION SENSOR

This work was performed under the direction of Dr. Hsiao-Wen Zan in the Organic Semiconductor Laboratory, Department of Photonics at the National Chiao Tung University in Hsinchu, Taiwan. The probing material, TPN-Cl_2, was provided by Dr. Chen-Hsiun Hung of Academia Sinica, Taiwan.

TPN-Cl_2 (meso-2,6-Dichlorophenyltripyrrinone) has been demonstrated as a highly sensitive and selective probe molecule for Zn ions, and has been blended within a hydrogel (polyHEMA) to provide excellent stability in a liquid environment. When Zn ions are captured by TPN-Cl_2, the resulting compound possesses a photoluminescence peak at 620 nm. Thus, in contrast to the work that was developed in the previous chapters – where the InGaZnO TFTs were passivated in order to allow for direct exposure to liquid – this chapter investigates the development and characterization of InGaZnO-based phototransistors on transparent glass substrates to capture the light emitted by TPN-Cl_2. The light sensitivity of both plain InGaZnO TFTs and InGaZnO/poly(3,3-didodecylquaterthiophene) (PQT-12) phototransistors is compared. Finally, integration of the full system successfully demonstrates the response to Zn ion concentrations of 1 mM.

7.1 Introduction

As the second most abundant transition metal ion in the human body, zinc (Zn^{2+}) plays a key role in determining the physiological condition. For example, high levels of Zn released in synapses contribute to selective nerve cell injury from stroke and from Alzheimer's disease [214–216]. Traditional Zn ion sensing films have predominantly been made from soluble materials or nanoparticles that can interfere with the natural biological processes of the body, and are therefore significantly invasive [217–219]. meso-2,6-Dichlorophenyltripyrrinone

(TPN-Cl_2), however, is a solid-state, liquid-stable and photoluminescent probe molecule that has been blended with a hydrogel polymer named poly(2-hydroxyethyl methacrylate) (poly HEMA), and has exhibits a photoluminescence intensity that is sensitive to Zn^{2+} ion concentrations [220]. Thus far, testing with this polymer has been accomplished using bulky bench-top optical characterization tools that are not practical for field deployment. In response, it is proposed that the attractive ability to fabricate InGaZnO TFTs on transparent glass be leveraged to capture the optical output of TPN-Cl_2 and consequently form a two-stage biochemical sensor.

7.2 System Overview

The envisioned system is shown in Figure 7.1. TPN-Cl_2 acts as the chemical sensing layer, while its intensity-modulated light output is captured by InGaZnO TFTs and converted to an electrical output signal. To improve the light sensitivity of InGaZnO TFTs, the addition of a photosensitive polymer, such as poly(3,3-didodecylquaterthiophene) (PQT-12), in order to form a phototransistor is investigated. A transparent glass slide is used as the platform for the entire system, as it will make it possible to isolate the TFT from the liquid, while the emitted light from the sensing film to pass through the bottom side and irradiate phototransistor on the top side. The photoluminescent sensing film works by emitting red light ($\lambda \approx 620$ nm) when excited by a blue laser ($\lambda \approx 420$ nm). It is the red light's intensity which is modulated by varying concentrations of Zn ions. In order to suppress the effect of the blue laser on the phototransistor, an optical bandpass filter is placed between the sensing film and the glass slide. When the red travels to the InGaZnO/PQT-12 interface, carriers are created and therefore a change in the phototransistor's drain current can be observed. This current is used as the sensor's output signal. Unlike the TFTs presented in previous chapters of this thesis, high-performance TFTs on glass were required here for integration. Ultimately, an integrated system on glass is proposed, which offers the advantage of being compact, light-weight and potentially more stable than a system where the TFTs are

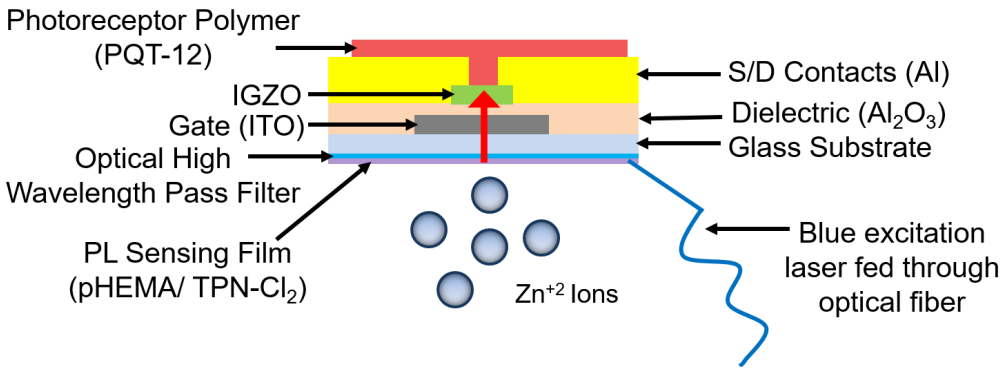
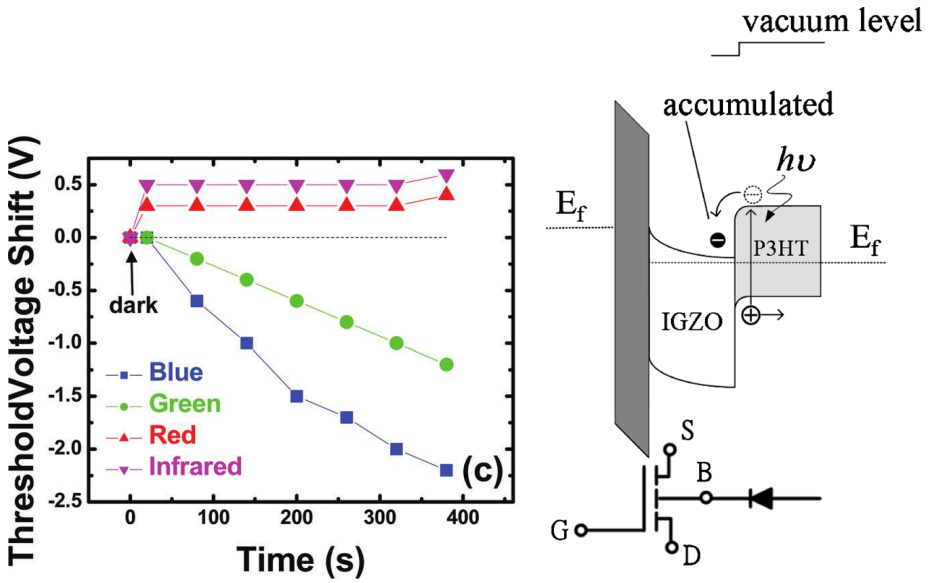


Figure 7.1. Cross-sectional image depicting the proposed sensing system. The presence of Zn^{2+} ions is detected by the photoluminescent sensing film. The emitted red light is transmitted through the glass substrate and modulates the current in the overlying InGaZnO/PQT-12 phototransistor.

directly exposed to fluid.

7.3 InGaZnO/Polymer Phototransistors

Due to the desire to use InGaZnO TFTs in flat panel displays, it was understood early on that the effect of light irradiance on these devices would have to be investigated. In 2008, the first systematic analysis of the wavelength- and intensity-dependent response of InGaZnO TFTs to light was published [221]. It was shown that the absorption properties of InGaZnO vastly differ from a-Si:H in the visible regime; this is indicated by the absorption coefficient which is measured to be one to two orders of magnitude lower. In UV wavelength range and below, however, the absorption coefficient of both InGaZnO a-Si:H increase rapidly. Consistent with this result, is the fact that as the wavelength of top-side irradiation decreased towards the UV range, the magnitude of the InGaZnO TFT's response, in the form of an increase in I_D and decrease in V_{TH}, increased. The other properties of the device, such as μ_{FE} and S, remained largely unaffected. As the intensity of the light was increased, the response also increased. Following this study, Professor HW Zan et al. at the National Chiao Tung University (NCTU) in Taiwan replicated similar results while examining the effect of bias conditions during illumination [222]. They found that illumination increases V_{TH} shift more for negative bias stress than for positive bias stress. The irradiation wavelength-dependent change of V_{TH} for unbiased and irradiated devices over time is



(a) (b)

Figure 7.2. (a) Threshold voltage (V_{TH}) shift over time upon exposure to different wavelengths of light. [222], (b) An energy band diagram of the phototransistor in saturation mode, showing how photons create new electron-hole pairs at the InGaZnO/P3HT interface. [43]

shown in Figure 7.2a. Professor Zan's team also demonstrated that the transformation of plain InGaZnO TFTs into phototransistors through the addition of a photosensitive polymer, such as poly(3-hexylthiophene) (P3HT), could help boost the response to white light [43]. It was claimed that the increased sensitivity to light in the phototransistor arises from the generation of excitons in the P3HT layer that dissociate at the interface between the InGaZnO and P3HT (Figure 7.2b). The built-in electric field generated by the difference in energy levels between the InGaZnO's conduction and the P3HT's LUMO level helps to readily inject electrons into the InGaZnO film. As electrons accumulate at the backside of the InGaZnO film, they induce a body effect which shifts the threshold voltage in the negative direction. The improved light-sensitivity of the phototransistor makes it an attractive device to sense the photoluminescent output signal of the TPN-Cl_2 sensing layer.

7.4 Zn Ion Photoluminescent Sensing Film

The Organic Semiconductor Laboratory under Prof. Zan's direction at NCTU has also undertaken work on developing Zn ion sensing films [220, 223]. The target behind this work is to reach a limit of detection below 10^{-6} M, since this is the typical concentration of Zn ions around a neural axon. Real-time detection (with samples taken every few minutes) is also desirable so that early detection of signs leading to stroke or Alzheimer's Disease can be achieved. Moreover, the sensor should be able to function not only in water, but also in complex aqueous biological media that contain various ions as well as biomolecules, such as proteins. Lastly, in order to avoid being invasive or harmful to those media, the sensor film was made in solid-state. This is unlike alternative sensing films that are dissolved in the analyte solution and can therefore disturb the systems under investigation.

The sensing film used is composed of two parts: the first is a fluorescent probe molecule named TPN-Cl_2 while the second is a host sol-gel polymer named poly(2-hydroxyethyl methacrylate), or pHEMA. For ease of use, the sensing mixture can be made into a planar film through simple spin coating and thermal curing. As seen in Figures 7.3a and 7.3b, Zn^{2+} concentrations down to 10^{-3} M can be detected successfully by observing an increase in the photoluminescence spectrum intensity at the peak wavelength over time. For comparison, the TPN-Cl_2-pHEMA was also synthesized as a fiber through the use of electrospinning. This approach has the advantage of increasing the surface area and therefore boosting sensitivity. The response of the sensing fiber to an ultra low Zn concentration of 10^{-6} M is shown in Figure 7.3c, where the fluorescence peak at 620 nm undergoes a steady and measurable increase in intensity over time. It should also be mentioned that in addition to being sensitive to Zn ions, TPN-Cl_2 has a further attractive property, which is its high selectivity. When tested with other prominent ions, such as sodium (Na^+) or potassium (K^+), it does not react as strongly as it does with Zn^{2+}. The intensity of the fluorescence is relatively small in pure DI water and, more importantly, it does not change over time. This indicates that the film is stable and will reduce the possibility of false positives.

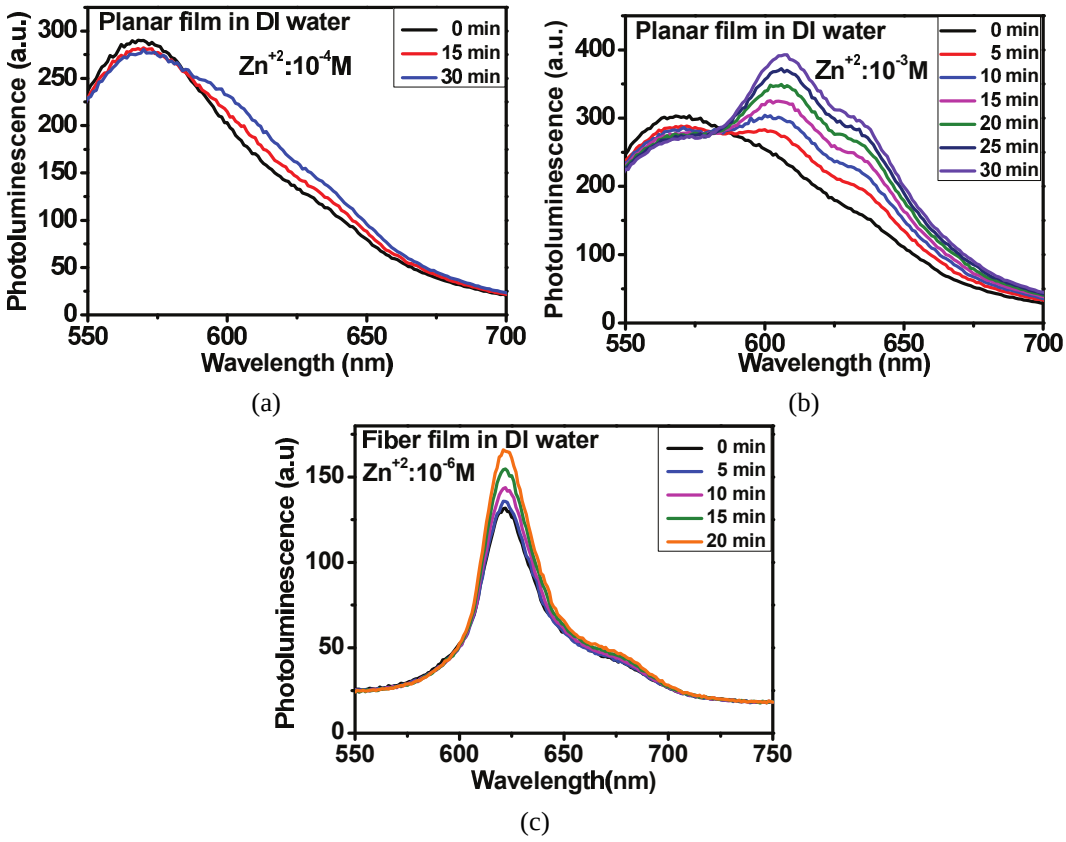


Figure 7.3. (a) Lack of change in photoluminescence spectrum response when the planar sensing film is exposed to a 10^{-4} M concentration of Zn^{2+} in DI water, (b) discernible PL peak intensity increase when the planar sensing film is exposed to a 10^{-3} M concentration of Zn^{2+} in DI water, (c) demonstration of improved sensitivity for the fiber sensing film compared to the planar film through demonstration of detection of 10^{-6} M concentration of Zn^{2+}. [220]

7.5 InGaZnO Phototransistor Fabrication and Electrical Characterization

The InGaZnO TFTs used in this work were fabricated at the NCTU cleanroom facilities, where a reliable fabrication process has been established using glass substrates [224]. This fabrication process is different from the fabrication process at Georgia Tech (Chapter 3) and is therefore presented here. As shown in Figure 7.1, the TFTs use a bottom-gate architecture. The glass substrates are initially received from Corning as 30 cm x 40 cm sheets. Since these are too large to be processed, they are then cut down to 3 cm x 3 cm slides. The glass sheets come with a pre-deposited 200-300 nm film of indium tin oxide (ITO). In order for the ITO layer, which is conductive, to be used as the bottom gate, it must be first

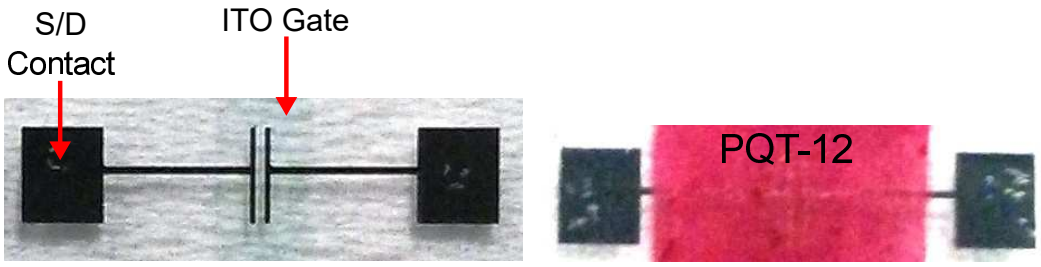
be patterned. This is accomplished by rolling on a dry photoresist, mounting the slide on a shadow mask and finally exposing it to ultraviolet (UV) light. After developing, the ITO is etched in a hydrochloric acid (HCl) that is heated to 60-70 °C. Following the etch, the sample is cleaned in DI water, acetone and isopropanol to remove the dry-film photoresist. However, due to the thickness of the photoresist, an additional oxygen plasma cleaning step is required to remove any remaining residue.

With the bottom gate contact formed, the next step involves the deposition of the gate insulator. Similar to the TFTs fabricated at Georgia Tech, aluminum oxide (Al_2O_3) is chosen due to its high dielectric permittivity and ability to be deposited via atomic layer deposition (ALD). In this case, a 50 nm thick Al_2O_3 layer is deposited at 200 °C. Furthermore, the good step-coverage of ALD allows the thick ITO gate to be completely isolated from the layers to be deposited next.

In order to define the active area, a shadow mask is attached to the glass slide. Then a 30 nm InGaZnO semiconducting film is deposited using RF sputtering at room temperature in an oxygen (O_2)/argon (Ar) atmosphere. The heavy Ar atoms are used to knock out atoms from the InGaZnO sputtering target while the partial partial pressure of O_2 is used to control the conductivity of the resulting film. The composition of the ceramic target is 1:1:1. A post-deposition anneal is also implemented at 400 °C for 60 minutes in an N2 environment.

The final step of the fabrication sequence involves the attachment of another shadow mask to define the source/drain (S/D) contacts of the TFT. Following this, the sample is placed in a thermal evaporation system to deposit the aluminum S/D metalization. The Al, whose melting temperature is lower than W's, evaporates and re-deposits on the cool surface of the glass slide above. The thickness of the S/D pads is 100-200 nm. A top-view image of the completed device is shown in Figure 7.4a. The width/length ratio of the TFT's channel is 1000 μm by 200 μm.

Using a probe station and an Agilent E5270B Precision Measurement Mainframe, the



(a) (b)

Figure 7.4. Top-view images of the (a) bare InGaZnO TFT on glass and (b) PQT-12 coated phototransistor.

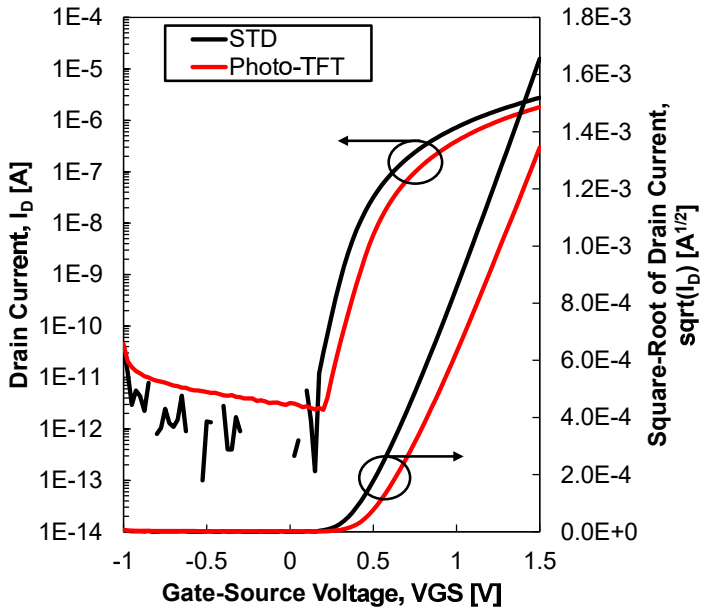


Figure 7.5. The transfer characteristic (I_D-V_{GS}) of the bare, or STD, (black) TFT in comparison to the PQT-12-coated phototransistor (red).

IV characteristics of the TFT were measured. In Figure 7.5, the transfer characteristic (I_D-V_{GS}) is shown for the both the STD (bare) device and the phototransistor to be discussed below. These TFTs have a V_{TH} between 0.15 and 0.2 V, which is significantly smaller than the glass-based TFTs presented in Section 3.5.1.1. The mobility, which is between 8 and 10 $cm^2\,V^{-1}\,s^{-1}$, is comparable to those devices fabricated at Georgia Tech.

To convert the InGaZnO TFT into a phototransistor, a photosensitive polymer must be added to the back-side of the device so that it interfaces directly with the InGaZnO film. Since most semiconducting organic polymers are p-type, this forms a pn-junction which is similar to a conventional photodiode. InGaZnO is transparent (i.e., it has a low absorption

coefficient) in the visible wavelength regime, which includes the fluorescence wavelength of the sensing film (620 nm). This means that the photosensitive polymer must be chosen to have a good absorption coefficient around 620 nm to complement the InGaZnO film. Though NCTU's OSL has previously demonstrated good results for the InGaZnO/P3HT phototransistor [43], this work has opted to work with PQT-12 in stead. The reason behind this decision lies with its chemical stability in air. P3HT was observed by Prof. Zan's students to degrade within days of being exposed to an oxygen atmosphere. PQT-12, on the other hand, continued to function for at least two weeks. This makes it a much more practical polymer to work with.

In terms of fabrication, the polymer film is added to the TFT through spinning in an N2-rich glove box. First, PQT-12, which comes in powder form from American Dye Source, must be dissolved in chloroform. The solution is then spun onto the glass slide to produce a film with 88 nm thickness. With reference to Figure 7.5, it can be seen that the electrical characteristics of the phototransistor differ, albeit slightly, from the STD TFT. For example, both the mobility and the on/off ratio decrease. Nonetheless, this device is still fully functional and can be tested for its photoresponse.

7.6 Light Sensing

In order to gauge the feasibility of a light sensing approach, a red (625 nm) light emitting diode (LED) with luminous intensity of 1150 mcd was used. The LED was mounted on the stage of a probe station, and a plastic cover was then placed above it to provide support for the glass substrate with the fabricated phototransistors. Each phototransistor was then probed from above in order to measure its I-V characteristics. The final configuration is shown in Figure 7.6. It should be noted that the probe station was located inside of a black box in order to exclude the effect of ambient light. Moreover, it should also be noted that this setup differs from the previously cited illumination studies [43, 221, 222] that investigated top-side illumination of InGaZnO TFTs fabricated on Si wafers. The use

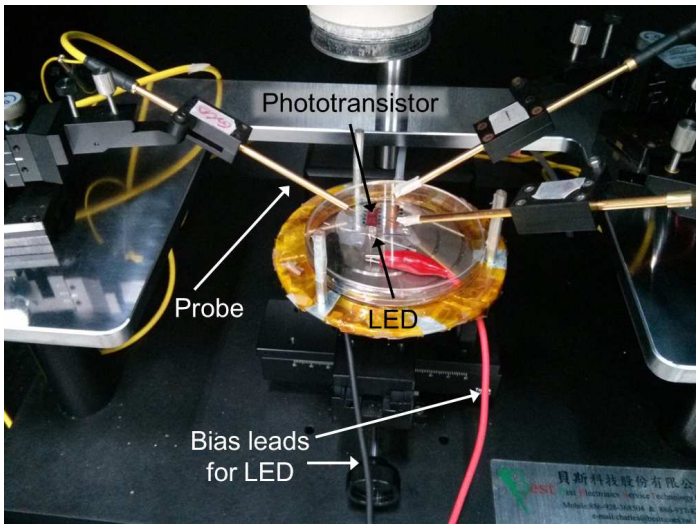


Figure 7.6. Measurement setup for light sensing

of a glass substrate will minimize the effect of reflections that might affect the Si-based experiments.

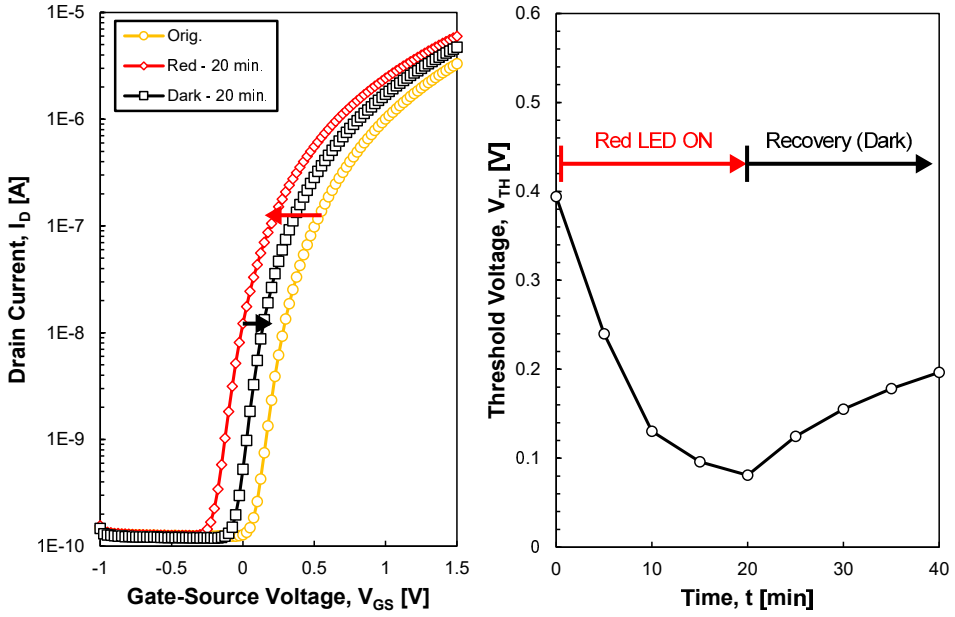
7.6.1 Control Experiments

In order to determine whether or not the PQT-12 polymer contributed to increased photosensitivity, the response of bare (STD) TFTs to different wavelengths was initially measured. In Figure 7.7, it can be clearly seen that exposure of the bare TFT to red light increases the current at a give V_{GS} or, in other words, induces a left-shift in the V_{TH}. Recovery after the LED is turned off is slow (i.e., asymmetric).

7.6.2 Phototransistor's Response to Light

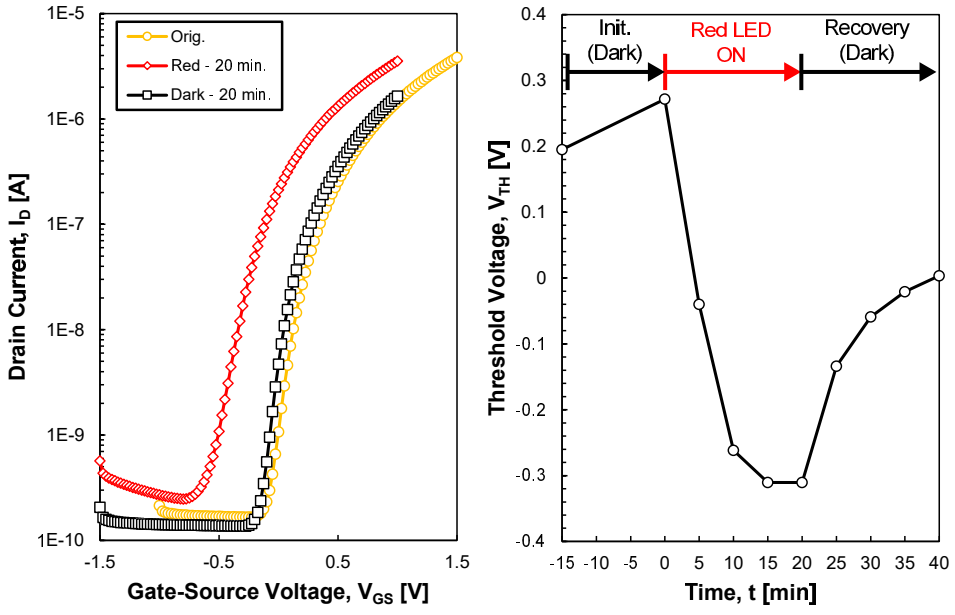
The phototransistor's response was then tested. In Figure 7.8, the response to red light alone is shown. Once again, the threshold voltage shifts negative. From the graph to the left, it can be seen that the off current of the phototransistor is comparatively larger than that of the bare TFT, particular in light-exposed cases. To mitigate the effect of ambient light prior to the beginning of testing, the chamber was closed 15 min prior so that the device could rest in the dark.

In Figure 7.9, a comparison is made between the response of the STD/Control device



(a) (b)

Figure 7.7. (a) I_D-V_{GS} sweeps conducted periodically on the STD device during either LED exposure or recovery. (b) Variation of the threshold voltage in the STD device over time; during $0 < t < 20$ min, the LED is on where as from $t > 20$ min, the LED is off.



(a) (b)

Figure 7.8. (a) I_D-V_{GS} sweeps conducted periodically on the PQT-12 coated device during either LED exposure or recovery. (b) Variation of the threshold voltage in the PQT-12 coated device over time; during $0 < t < 20$ min, the LED is on whereas from $t > 20$ min, the LED is off (recovery).

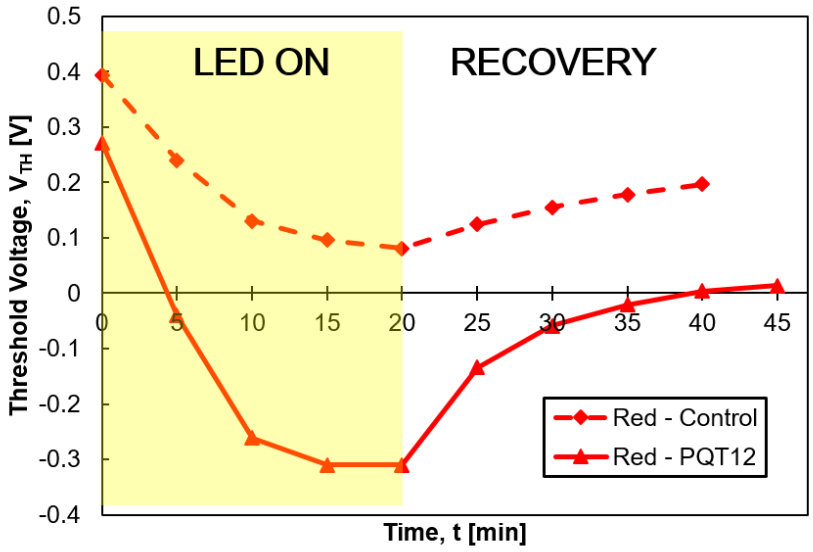


Figure 7.9. Comparison of the STD device's threshold variation in response to red versus that of the PQT-12 coated device.

versus that of the PQT-12 covered device (i.e., the phototransistor). It is now clear that the phototransistor is more sensitive to red light than the bare TFT. It was calculated that $\Delta V_{TH,STD} = 0.40$ V, while $\Delta V_{TH,PQT\text{-}12} = 0.53$ V. Though a 130 mV difference may not seem significant, one must consider that the drain current – not V_{TH} – is what will be monitored in real-time during sensing. Therefore, degree of current amplification after 20 minutes of exposure to red light when $V_{GS} = V_{TH,original}$ was calculated:

$$\frac{I_{red,STD}}{I_{0,STD}} = 8.34$$

$$\frac{I_{red,PQT-12}}{I_{0,PQT-12}} = 14.14$$

As a result, there is a 70% increase in the drain current change due to irradiation to red light.

7.6.3 PQT-12 Stability

The response of the phototransistor to red light was measured over a three week period in order to verify its stability. As shown in Figure 7.10, during the first two weeks, ΔV_{TH} remains almost constant (i.e., $\Delta V_{TH} \sim 0.5$ V). However, during the 3rd week $\Delta V_{TH} = 0.31$

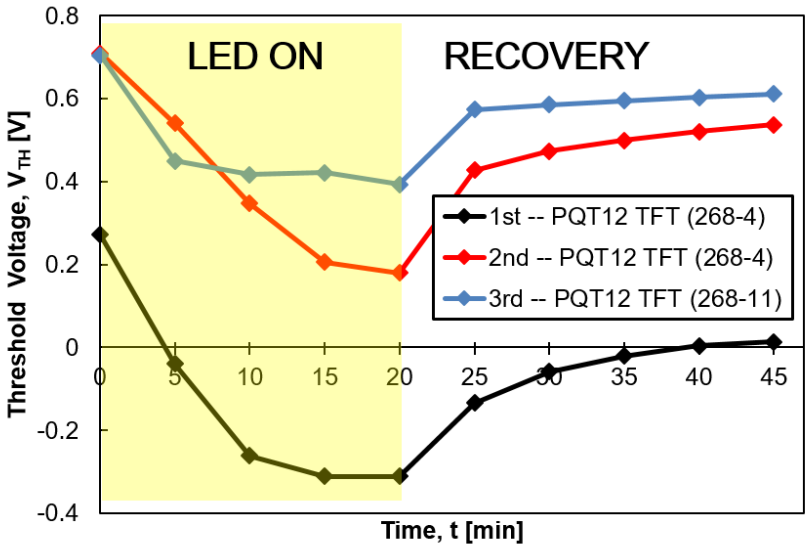


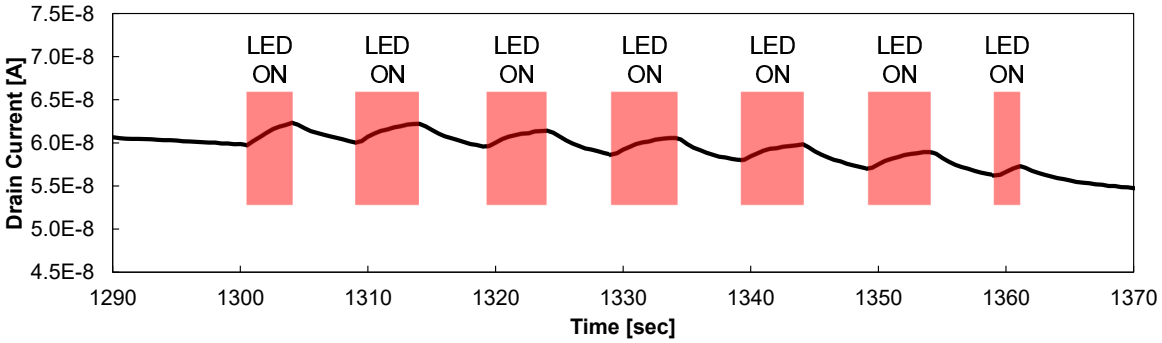
Figure 7.10. Comparison of the PQT-12 device's threshold variation in response to red light over a 3-week period.

V. Since this is comparable to the response of the bare TFT, it can be deduced that the PQT-12's effectiveness has broken down and the response is dominated by the InGaZnO film itself. The difference in the original threshold voltage between the 1st and 2nd weeks can be explained by the length of time that the devices were left to rest in the dark prior to the beginning of testing.

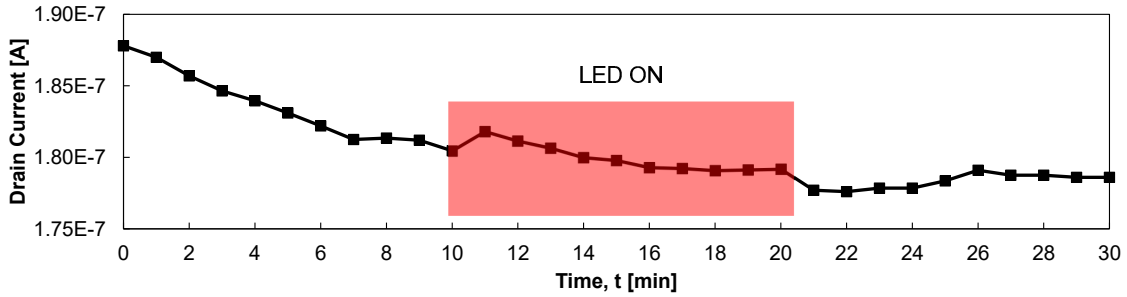
7.6.4 Transient Response of the Phototransistor to Red Light

Continuous measurements were also carried out in order to better observe the response time for these sensors, as well as their repeatability. In Figure 7.11a, the phototransistor was subjected to the same LED light source as that used in the above experiments. In this case, the LED was switched on and off with a period of 10 sec and a duty cycle of 50%. It is clear that the phototransistor's response is both significant and repeatable over time. In addition, for such short exposure times, recovery seems to very rapid. It should be noted that the bias point for this experiment was chosen such that $V_{GS} \sim V_{TH}$.

Figure 7.11b shows another experiment where the LED's brightness was calibrated to match that of the sensing film's output for a Zn ion concentration of 10^{-3} M. Since Zn ion



(a)



(b)

Figure 7.11. (a) Transient response of the phototransistor to bright red light; the bias point for this test is V_{GS} = 1.3 V and V_{DS} = 2 V. (b) Transient response of the phototransistor to dim red light (intensity of which is comparable to sensing film's output with Zn concentration of 10^{-3} M); the bias point for this test is V_{GS} = 0.5 V and V_{DS} = 2 V.

concentration fluctuations in the body take place over a period of minutes, the phototransistor's current was sampled once every minute and the red LED was turned on for a total of 10 minutes. Once again, an increase in current during the on window is measured, while a decrease in current is recorded once the light is turned off. The overall downward trend of the current over time is due to bias stress (see Section 4.3).

7.7 System-Level Validation

The above measurements used an LED light source that acted as a surrogate for the photoluminescent TPN-Cl_2 sensing film, and permitted repeatable characterization of the light response of the phototransistor/TFT. Motivated by the promising results in Figure 7.11b, the full system (as shown in Figure 7.1) was integrated to evaluate if the phototransistor could sense the actually emitted light from the TPN-Cl_2 film when exposed to a liquid

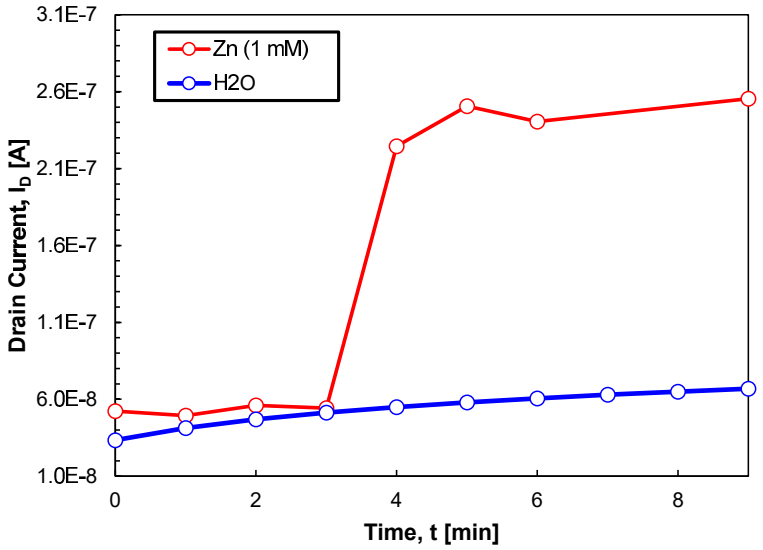


Figure 7.12. Response of entire system to H_2O (blue) and 1 mMol solution of Zn^{2+} ions (red).

containing Zn ions.

The results of this initial characterization are shown in Figure 7.12. As a control, the sensor was exposed to DI water first. After 10 minutes, no significant rise in the drain current was found and therefore confirms the stability of the sensor. However, when 10^{-3} M of Zn^{2+} was introduced, a discernible increase in the phototransistor's I_D was recorded. This change corresponds to the increase in the PL intensity of the pHEMA/TPN-Cl_2 sensing film.

7.8 Conclusion

The above experiments have investigated the development of a bottom-illuminated InGaZnO/ PQT-12 phototransistor on glass for use in an integrated Zn ion sensor system. This involved successfully fabricating semi-transparent InGaZnO TFTs on glass, then converting them into phototransistors through the addition of a spin-coated layer of photo-sensitive PQT-12 polymer. It was shown that the phototransistor's response to red light is 70% larger than that of the bare TFT. Transient measurements of the phototransistor's response to red light were also completed, demonstrating that the device does exhibits a repeatable and rapidly observable response to light irrandiance. Lastly, system-level integration was

successfully achieved for the first time, demonstrating a detectable response for Zn ion concentrations of 10^{-3} mol. Further work in this area will focus on lowering the limit of detection, and investigating the use of the fiber-based sensing film rather than the planar film used thus far.

CHAPTER 8

A FEASIBILITY STUDY OF FLIP-CHIP PACKAGED GALLIUM NITRIDE HEMTs ON ORGANIC SUBSTRATES FOR WIDEBAND RF AMPLIFIER APPLICATIONS

Gallium nitride (GaN) technology has emerged as a front-runner for high power electronics applications. Due to the large thermal dissipation of GaN devices and circuits, present-day packaging strategies have focused on the use of expensive materials with high thermal conductivity, such as aluminum nitride (AlN), while low-cost organic materials, such as liquid crystal polymer (LCP), have been overlooked. In this chapter, the aim is to establish the thermal and electrical operating limits of packaged GaN devices on organics. Dies that were wire-bonded on AlN showed best performance, and were able to dissipate more than 6W of power while remaining below the maximum operating junction temperature. On the other hand, flip-chip bonded devices on LCP were severely limited by thermal effects, even at a 10% duty cycle. This study motivates the need for advanced packaging techniques, such as integrated microfluidics or backside heat-sinking, in order to make LCP a viable material for high-power applications.

8.1 Introduction

For state-of-the-art performance, GaN monolithic microwave integrated circuits (MMICs) on silicon carbide (SiC) substrates have been preferred, since they offer low parasitics, which enable wide bandwidth designs, high scalability and excellent thermal management due to SiC's high thermal conductivity [96, 225]. The drawback of MMICs, however, is that they are costly and require more time to manufacture compared to hybrid systems. If a hybrid approach is taken, the GaN HEMTs are usually wire-bonded on brittle ceramic substrate materials (e.g., alumina), or bulky carriers made from copper (Cu) or other copper-based alloys [22, 226]. Though this approach yields optimum thermal performance

by leveraging the high thermal conductivity of these carriers, the use of wire-bonds introduces high interconnect parasitics (i.e., inductance) which greatly limit the achievable bandwidth of PAs assembled in this manner.

An alternative packaging method to wire-bonding is the flip-chip bond technique, which minimizes the interconnect length by replacing wire-bonds with short metallic bumps and, in turn, improves the bandwidth. Flip-chip bonded wideband GaN PAs have already been demonstrated on aluminum nitride (AlN) due to its high thermal conductivity [94, 95], but the limitations of this packaging scheme have not been studied in detail and reported. Despite its advantages, AlN poses a relatively high cost and mechanical fragility, which might limit its suitability for rugged or portable applications.

To address these issues, low-cost organic packaging materials have been widely investigated in recent years for high-frequency electronics. A prominent example is liquid crystal polymer (LCP), which has now been characterized up to 170 GHz [108], showing a low dielectric constant (ϵ_r = 2.95) and low loss tangent (tanδ = 0.0025). Moreover, it has a coefficient of thermal expansion (CTE) that matches that of copper and a low melting temperature that enables multilayer and embedded systems-on-package (SOP). Thus far, CMOS [114], silicon-germanium (SiGe) [115] and gallium arsenide (GaAs) amplifiers [227] have all been successfully flip-chip bonded on LCP. Though one study presented a wire-bonded GaN transmitter module on LCP [228], a flip-chip bonded amplifier on LCP has yet to be demonstrated.

The purpose of this work, therefore, is to evaluate the feasibility of flip-chip bonding high power GaN high electron mobility transistors (HEMTs) on organic substrates, particularly LCP, and to identify performance limits given LCP's poor thermal conductivity. Since maximum power is dissipated at DC, pulsed IV curves at different duty cycles will be used to evaluate the thermal impact of this packaging on the electrical performance of the GaN HEMTs. This technique is coupled with the use of infrared (IR) spectroscopy to

quantify the maximum temperature on the die during operation. In order to provide context for this study, three further packaging schemes are also compared: (1) wire-bonded on AlN (WB-AlN), (2) flip-chip bonded on AlN (FC-AlN) and (3) wire-bonded on LCP (WB-AlN).

8.2 Design

8.2.1 Cree Inc. GaN Die (CGHV1J006D)

To ensure a fair comparison across all packages, the same commercially-available GaN HEMT from Cree Inc. is employed: the CGHV1J006D [229] (Figure 8.1). This 800 μm × 840 μm bare die, which is fabricated using Cree's GaN-on-SiC process with a 0.25 μm gate length and 1.2 mm gate periphery, is characterized by a typical saturation power (P_{SAT}) of 6 W and drain bias of 40 V. Absolute ratings include a maximum operating junction temperature ($T_{J,max}$) of 225 °C, maximum drain current of of 800 mA and maximum drain voltage of 100 V at 25 °C. Through-SiC vias provide a backside gold-plated ground contact, thus eliminating the need for source wire-bonds. For reference, if the die is attached to a 40 mil thick copper-molybdenum-copper (CuMoCu) carrier using 80/20 gold-tin (Au-Sn) solder, the maximum dissipated power (P_{diss}) is 7.2 W.

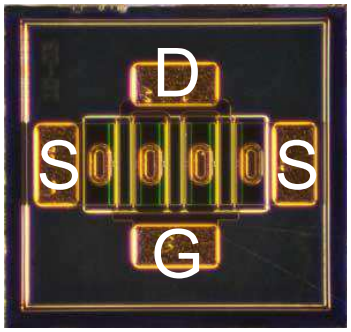


Figure 8.1. Top-view photograph of CGHV1J006D GaN-on-SiC die from Cree.

8.2.2 Package Layouts

In order to facilitate testing, it was important to make the packages directly probe-able. Therefore, coplanar waveguide (CPW) lines were chosen for compatibility with high-frequency ground-signal-ground (GSG) probes. The signal line width and gap were limited by the width of the gate and drain contact pads (200 μm) as well as and the pitch from gate/drain to source pads (approx. 290 μm). For the wire-bonded package (Figure 8.2a, the two ground planes were connected to form a contact pad to which the die's bottom-side source was attached. To ensure alignment between the die's pads and the flip-chip package's pads for bonding (Figure 8.2c), particular attention was given to the location of the contact pads, which do not sit at the edge of the die. Vias were also dispersed throughout the ground planes in order to ensure a common ground for the top and bottom metallization.

8.3 Fabrication and Assembly

8.3.1 Aluminum Nitride (AlN) Board Fabrication

The ground vias were first drilled through a bare 15 mil thick AlN board using a CO_2 laser. A 5 μm thick Au film was deposited onto the top and bottom of the board through sputtering, which also coated the via sidewalls. The top side was then patterned through a photolithographic process.

8.3.2 Liquid Crystal Polymer (LCP) Board Fabrication

A 4 mil thick LCP substrate from Rogers Corporation was used. The double-clad copper was stripped from the top side only using nitric acid etchant. A CO_2 laser was then used to drill 4 mil diameter vias. Subsequently, a 5 μm thick film of copper was redeposited onto the top side using a DC sputterer, which also served to metallize the via sidewalls. In order to protect the metalized vias adequately, a Suss AltaSpray Spray Coater was used to deposit photoresist for lithography.

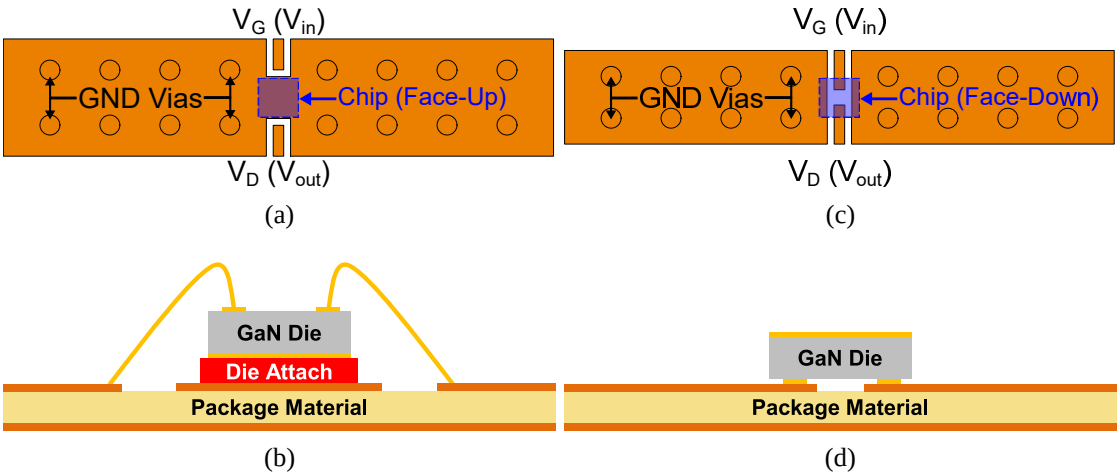


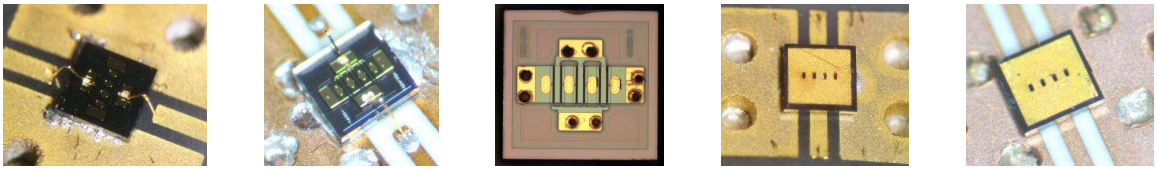
Figure 8.2. Traditional package interconnection strategies: Wire-bonding (a) layout and (b) cross-section, Flip-chip bonding (c) layout and (d) cross-section.

8.3.3 Wire-bond Packaging

For the wire-bond on AlN (WB-AlN) package, the die was attached to the gold pad using a 97/3 indium-silver (InAg) ribbon solder from Indium Corporation whose liquidus temperature is 143 °C. Since the WB-LCP sample was metalized with copper, a eutectic bond was not possible. Therefore the die was attached using silver epoxy, a method which has commonly been used thus far for LCP-based packages. Following the die attach step, the gate and drain pads were wire-bonded using a wedge tip and 1-mil diameter gold wire. A cross-section of the wire-bond package is shown at the top of Figure 8.2b. Figures 8.3a and 8.3b depict the fully packaged wire-bonded devices.

8.3.4 Flip-Chip Packaging

In order to minimize parasitics and facilitate heat transfer, two Au bumps (40 μm tall) were applied to each pad on the Cree die (see Figure 8.3c). This was done using an Au wire ball bumper that combines thermo-compression and ultrasonic energy. A Finetech Submicron Flipchip Bonder was used to align and thermally compress the chip to either the AlN or LCP substrate. To help reinforce the bond between the gold bumps and the package, a controlled dose of silver epoxy was also used. The completed flip-chip packaged devices are shown in Figures 8.3d and 8.3e.



(a) (b) (c) (d) (e)

Figure 8.3. Pictures of packaged 6 W GaN-on-SiC HEMT die: (a) wire-bonded on aluminum nitride, (b) wire-bonded on LCP, (c) stud bumped die prior to flipping, (d) flip-chip bonded on aluminum nitride, and (e) flip-chip bonded on LCP.

Table 8.1. Overview of thermal conductivity of materials

Role	Material	Thermal Conductivity [W m^{-1} K^{-1}]
Die Materials	SiC	370
	GaN	130
	AlGaN	19
Package Materials	LCP	0.2
	AlN	180
Package Metallization	Cu	400
	Au	310
Die Attach	Silver Epoxy	2.5-29
	InAg	72

8.3.5 Overview of Materials

Table 8.1 provides an overview of the thermal conductivity of the various materials that were used during the fabrication and packaging process. The materials are categorized depending on their role in the system. It is important to note that both the package substrate material (LCP vs. AlN) as well as the die attach material (silver epoxy vs. InAg) play a vital role in influencing the thermal management of the package.

8.4 Experimentation

Both pulsed IV curves and IR thermal images were obtained on a QFI InfraScope II system (Figure 8.4a). 500 um pitch GSG probes from GGB Picroprobe were used to probe the devices. Short fixture cables on both the input (Gate) and output (Drain) sides connected the probes to Agilent Bias Tees (Model No. 11612A with High Current 001 option). In

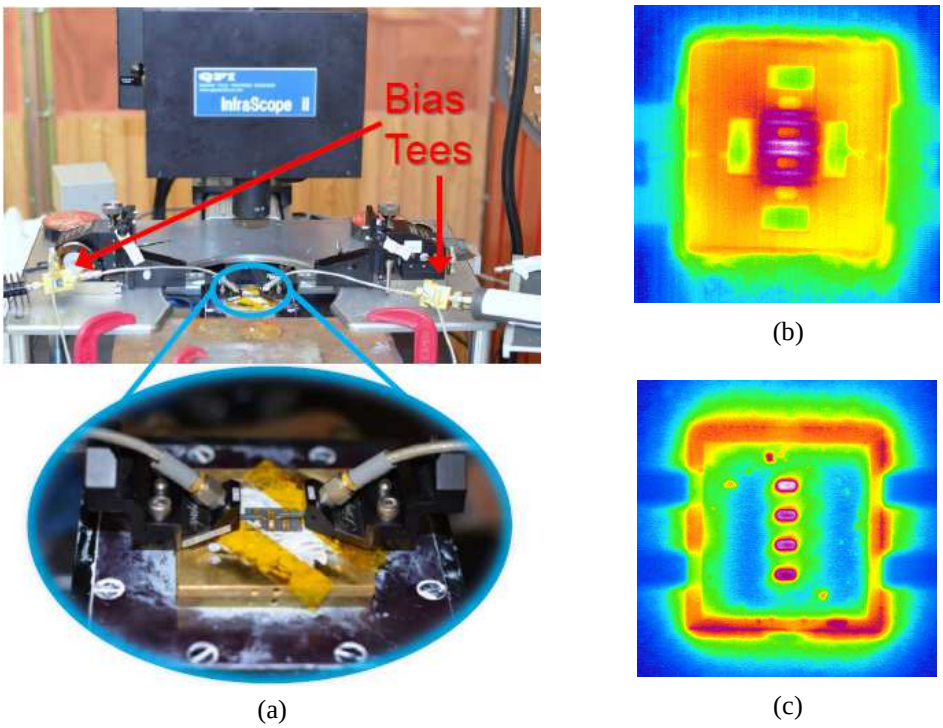


Figure 8.4. (a) IR images captured of (b) wire-bond and (c) flip-chip packages.

order to ensure device stability throughout testing, 50 Ω terminations were also connected to the RF input ports of the bias tees. An AMCAD Pulsed IV system operated through Maury Microwave's IVCAD software was used to bias the devices. This system is capable of sourcing up to 20 A at 250 V and can provide pulse widths as short as 200 ns. For these tests, a 50 μs period was chosen along with three different duty cycles (δ): 10% (5 μs drain pulse width), 20% (10 μs drain pulse width) and 50% (25 μs drain pulse width). It should be noted that the stage of the QFI system was maintained at 60 °C throughout all testing. To provide a good thermal contact from the stage to the package, thermal paste was applied.

8.5 Results

8.5.1 Thermal IR Imaging

The goal of using IR imaging was to determine the maximum temperature (T_{max}) on the die under different operating conditions and, in turn, identify the range of bias points (or

dissipated powers) that would allow the device to function below the abovementioned maximum operational junctional temperature of 225 °C given by Cree Inc. Each package was tested under different duty cycles and a fixed drain bias (V_{DS}) of 20 V. The dissipated power (P_{diss}) was adjusted through changes to the drain current (I_D), which itself was controlled by the gate voltage (V_{GS}) given the fixed V_{DS}. In this experiment, two values for P_{diss} were calculated: peak dissipated power ($P_{diss,peak}$) which is defined as $I_D \times V_{DS}$ during the pulse, and average dissipated power, which is defined as the peak dissipated power multiplied by the duty cycle ($P_{diss,avg} = P_{diss,peak} \times \delta/100$).

Examples of the captured IR images are shown in Figures 8.4b and 8.4c. In this case, the WB-AlN device was biased at V_{DS} = 20 V, I_D = 329 mA at δ = 50%, corresponding to $P_{diss,peak}$ = 6.56W and $P_{diss,avg}$ = 3.28 W. A peak temperature of 104.2 °C was registered, as expected, in the middle of the die where the fingers of the HEMT are located. Out of the four vertical source vias, it can be seen that the central ones, which are located within the hotspot, are the hottest. Due to the die's orientation in the FC-AlN package, it was only possible to obtain thermal information about the backside of the device. The image of the FC-AlN package in Figure 8.4c was taken for a bias condition of V_{DS} = 20 V and I_D = 103 mA at δ = 50%. At $P_{diss,peak}$ = 2.06W and $P_{diss,avg}$ = 1.03 W, the T_{max} was 93.8 °C. Interestingly, T_{max} was recorded within the four vias, signifying that they indeed play a critical role in dissipating the heat away from the active region of the device located on the reverse side of the die.

IR images were collected for each of the packages over a range of dissipated powers and duty cycles in order to determine what range of bias points would cause the device to approach temperatures that could be detrimental to its function (approximately 200 °C). Figure 8.5a) contains a plot of $P_{diss,avg}$ vs. T_{max} for the two WB packages at different values of δ. Given the vastly superior thermal conductivity of AlN over LCP, it came as no surprise to see that the WB-LCP package reached these higher temperatures at significantly lower dissipated powers compared to the WB-AlN package. In fact, at δ = 10% and 20%,

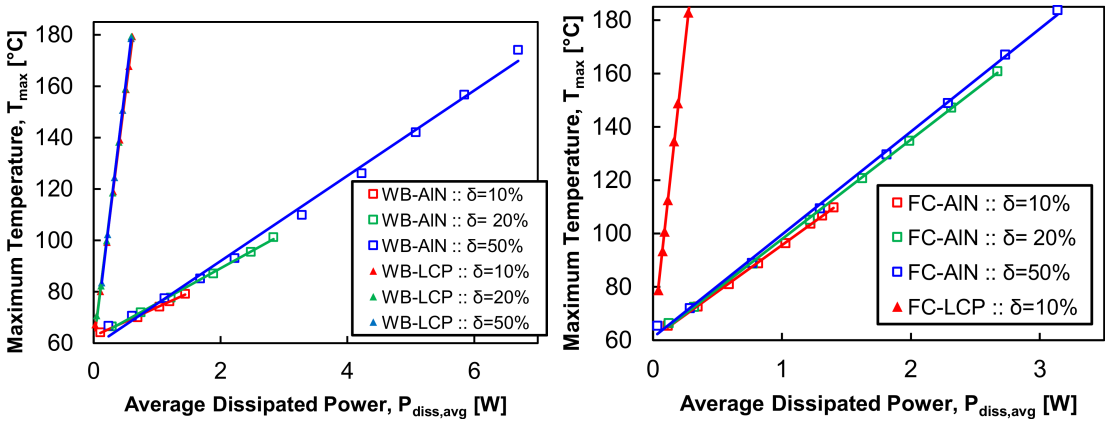


Figure 8.5. Thermal resistance curves extracted from the (a) wire-bonded, (b) flip-chip bonded packages.

the performance of the WB-AlN package was not limited by T_{max}, rather it was the peak current (800 mA) that determined the upper limit of testing. The WB-LCP package reached T_{max}>180 °C below $P_{diss,avg}$ = 1 W. To quantify this trend, the total thermal resistance (R_{TH}) was determined for each package by drawing a line through each set of data and extracting the slope.

The analogous comparison for the flip-chip packages was made in Figure 8.5b, demonstrating, once again, the superior thermal performance of AlN. Due to rapid heating in the FC-LCP package, it was only tested at δ = 10%, where T_{max} > 180 °C was reached at $P_{diss,avg}$ < 500 mW, thus greatly limiting this type of package for real-life circuit implementation. In addition to a dependence on the package materials, the data show that, for all packages, R_{TH} is also a function of the duty cycle. Finally, it should be noted that each line intersects with the y-axis at 60 °C, which relates to the base plate temperature that was maintained through the tests.

Table 8.2 summarizes the performance limitations of each package. Given the 6W rating for this device, it can be concluded that, when operated under the pulsed conditions that were considered here, all of the AlN-based packages are capable of reaching the necessary peak power levels. On the other hand, the LCP packages are very limited in use, such that

Table 8.2. Overview of the thermal performance for the various packages.

Package	R_{TH} [°C/W]	$P_{diss,avg}$ at T_{max} = 180 °C [W]	$P_{diss,peak}$ at T_{max} = 180 °C [W]
WB-AlN			
δ = 10%	11.19	10.73*	100.72*
δ = 20%	13.61	8.81*	44.05*
δ = 50%	18.61	6.61	13.22
WB-LCP			
δ = 10%	193.41	0.62	6.2
δ = 20%	199.75	0.6	3.0
δ = 50%	204.98	0.59	1.17
FC-AlN			
δ = 10%	34.87	3.44*	34.4*
δ = 20%	37.31	3.22*	16.1*
δ = 50%	38.57	3.11	6.22
FC-LCP			
δ = 10%	440.47	0.27	2.72

*Extrapolated from measured data.

only the WB-LCP package operated at δ = 10% reaches >6W peak power. It should be noted that with proper matching for these packages in order to achieve maximum power added efficiency (PAE), the dissipated power can be reduced, thus widening the potential for the LCP packages. All in all, however, the FC-LCP package is severely limited in its use, with extremely high temperatures being recorded even at $P_{diss,peak}$ = 2.72W at δ = 10%.

8.5.2 Pulsed IV Curves

From the IR measurements, maximum power compliance levels (see Table 8.2) were extracted which could be defined in IVCAD to safely perform pulsed IV sweeps. This is similar to defining a load-line. In Figure 8.6a, the output characteristic (V_{DS} vs. I_D) for the WB-AlN package is plotted under pulsed conditions for various duty cycles and values of V_{GS}. It is observed that as the duty cycle rises, heat effects come into play, which lead to a drop in the saturation current. This phenomenon is especially prominent at higher current levels; at low values of V_{GS} the difference from δ = 10% to 50% is not significant. In Figure 8.6b, similar IV curves are plotted for the FC-AlN package. Here, as expected, the more rapid increase in temperature due to the higher R_{TH} of this package leads to more noticeable

falls in current. When compared to the WB-AlN package (Figure 8.6c), it is clear that the WB-AlN package is superior to the FC-AlN package. At δ = 10%, the two curves overlap, showing little difference in performance between the two packages. However, as δ is increased to 50%, the measured saturation current drops off faster in the FC-AlN package than for the WB-AlN package.

Figure 8.6d shows the IV curves for the WB-LCP package. Due to the temperature and power limitations identified with the IR camera the characteristics were only measured at lower current levels to avoid damaging the device. Despite this lower range of operation, the effects of heating are clear to be seen. Measurements on the FC-AlN package were only conducted for δ = 10% (Figure 8.6e). Even under these conditions, there are clear aberrations in the IV curves which confirm that this package would not be suitable for high-power applications, which are typically well-suited to GaN. A comparison between the two LCP packages in Figure 8.6f, shows the extent to which the performance of the device degrades when it is flip-chip bonded on LCP: not only does the current fall at this low duty cycle of operation, but the knee current is also lower than in its wire-bonded counterpart.

8.6 Conclusions

This work has studied the thermal and electrical performance of GaN HEMTs packaged in AlN and LCP, with either wire-bonding or flip-chipping methods. Devices that were wire-bonded on AlN fulfilled their 6W rating, thus demonstrating that this package does not impose thermal restrictions on the device's performance. Devices wire-bonded on LCP, however, showed significant degradations in performance, such that 6Wwas only achieved at δ = 10%. Flip-chip bonded devices on AlN showed favorable performance, with more than 6W of power capable of being dissipated, even at δ = 50%. Finally, when the die was flip-chip bonded on LCP, severe performance limitations were identified, whereby a maximum average dissipated power of only 0.27W could be handled without surpassing

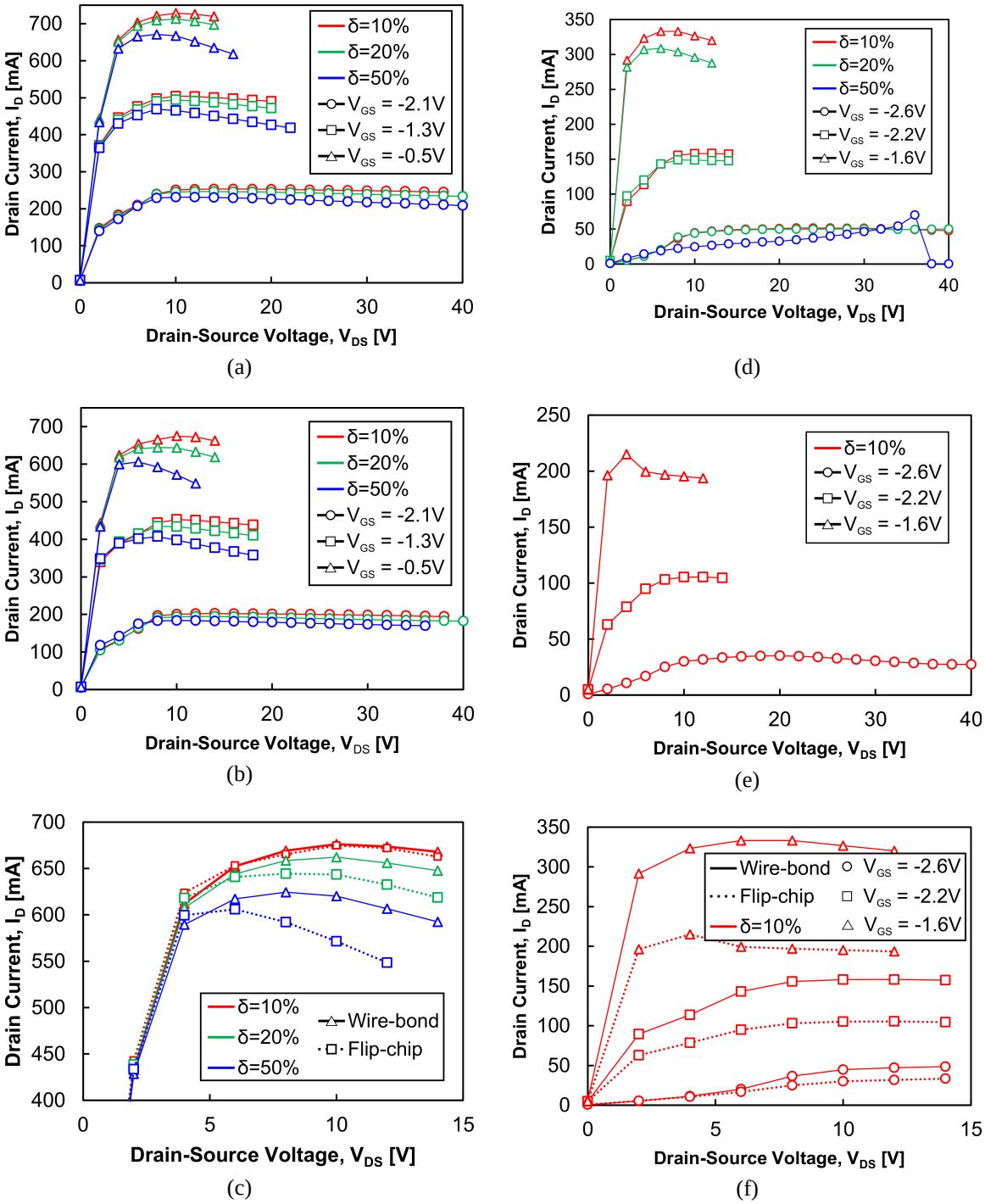


Figure 8.6. I-V sweep measurements on each package: (a) WB-AlN, (b) FC-AlN, (c) WB vs. FC on AlN, (d) WB-LCP, (e) FC-LCP, (f) WB vs. FC on LCP

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the maximum junction temperature of 225 °C specified for the device.

In conclusion, though flip-chip packaged devices make it possible to extend the bandwidth of hybrid GaN PAs, the thermal implications of not providing a heat sink to the bottom side of the die cannot be ignored. Therefore, in order for flip-chipping – particularly on organics – to become feasible for GaN modules, further studies should be carried out. Possible avenues include: (1) the development of a multilayer package incorporating a high thermal conductivity heat sink for the otherwise floating bottom side (2) integrated microfluidics [230] or (3) optimized use of thermal vias [231].

CHAPTER 9

A 5.4 W X-BAND GaN POWER AMPLIFIER IN AN ENCAPSULATED ORGANIC PACKAGE

Gallium nitride (GaN) amplifiers are inherently well suited for high power applications, but their increased power densities call for high thermal conductivity (*k*) substrates, such as copper (Cu) or aluminum nitride (AlN), to provide adequate thermal management. Thus, low-cost/low-k substrates, such as organics, have been traditionally passed over for GaN-based amplifiers, despite their advantageous high-frequency characteristics. In this paper, an encapsulated package is investigated to circumvent the thermal limitations of liquid crystal polymer (LCP), one such organic, while leveraging its multilayer and low-loss nature. An X-band GaN PA in such a package has been designed and fabricated, showing a PAE of 38% and P_{SAT} of 5.4W under CW operation, or 49% PAE and 7W P_{SAT} at 50% duty cycle.

9.1 Introduction

As mentioned previously, flip-chip bonding offers the advantage of reduced interconnect inductance in comparison to wire-bonding [232]. This can be visualized from the plot of S_{11} shown in Figure 9.1, where the response of a wire-bonded and flip-chip bonded die on AlN are compared. The rotation of S_{11} around the Smith Chart is larger for the wire-bonded device, making it more difficult to realize a wide-band matching network for a hybrid power amplifier. Despite the advantages for microwave design, the results presented in Chapter 8 demonstrate that a more sophisticated package must be designed for flip-chip bonding high power GaN devices, especially on organic substrates with low thermal conductivity (*k*).

In response to this need, this chapter presents a novel embedded GaN packaging technique on LCP. Though encapsulated packaging in LCP has been demonstrated for both GaAs and SiGe chips previously [114, 116] both reports used thick bottom substrates that left the die's backside unconnected. This poses a major threat to the reliable operation of

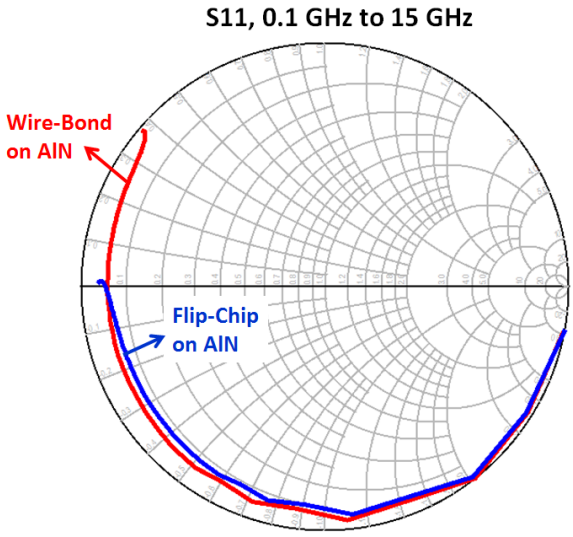


Figure 9.1. Input reflection coefficient (S_{11}) of the GaN HEMTs from 100 MHz to 15 GHz when packaged by flip-chip bonding and wire-bonding on AlN.

high-power GaN devices. In this work, organic laminates of suitable thickness are selected so that a heat sink can be introduced to the backside of the device. All in all, the encapsulated packaging approach offers several benefits: 1) thermal management unconstrained by LCP since the die is attached to copper heat sink, 2) low interconnect parasitics since flip-chipping, instead of wire-bonding and 3) protection of the die from harsh environments provided by LCP's near hermetic nature. Characterization of the novel package demonstrates that, for the first time, continuous-wave (CW) DC operation is possible for GaN on organics. Following from this result, the full RF potential of the concept is validated through the design, fabrication and characterization of an X-band PA.

9.1.1 Design and Implementation of the Encapsulated Package

The encapsulated package, shown in Figure 9.2, is composed of five layers (top to bottom): top metal (M1), top LCP substrate (S1), bottom metal (M2), bottom LCP substrate (S2) and a thin 1 mm thick copper heat sink (M3). A bare 0.25 μm GaN-on-SiC high electron mobility transistor (HEMT) die from Cree (CGHV1J006D) is packaged within a cavity formed in the S2 layer. Since the die is 100 μm thick, the S2 layer was chosen to be 7 mil (175 μm) thick for full encapsulation. The backside of the die is attached to a copper heat

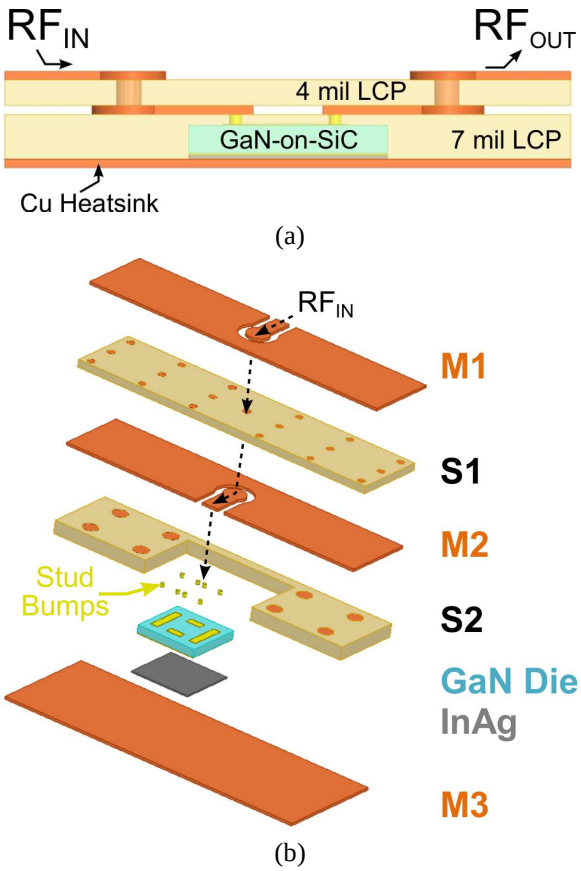


Figure 9.2. (a) Cross-section of the encapsulated package in organics for GaN devices and circuits, (b) exploded view of the package.

sink using an indium silver (InAg) solder ribbon, while stud bumps on the top-side pads connect it to the M2 layer. No underfill between the die and M1/S1 is used in this work. A through-LCP via transition in the S1 layer connects M2 to M1. The via inductance was minimized by reducing the S1 thickness to 4 mil. Ground vias are also present to connect the grounds across all levels.

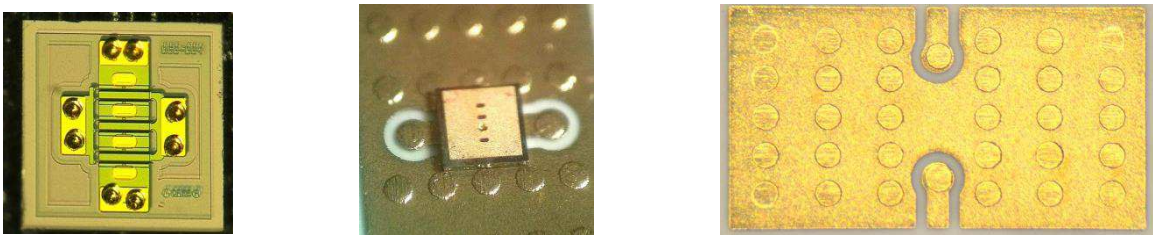
A probe-able 50 Ω coplanar waveguide (CPW) with a signal width and gap of 200 μm and 100 μm, respectively, was designed in both the M1 and M2 layers using Ansys HFSS. The signal line width was chosen to match the 200 μm width of the die's gate and drain contact pads. The top and bottom-side via catch pads were further tuned to minimize losses. This resulted in simulated insertion loss below 0.15 dB up to 20 GHz and return loss above 20 dB over the same band.

9.1.2 Fabrication of the Encapsulated Package

Fabrication of the top board (M1, M2, and S1) consisted of via drilling, electroless plating, patterning of the photoresist, patterned plating and finally etching the metal layers. A thick gold finish was applied to the board in order to enable thermo-compression flip-chip bonding of the die. For the bottom substrate, a CO_2 laser was used to drill the cavity and ground vias. Metallization and patterning were subsequently accomplished in tandem using a shadow mask and a copper sputtering step.

InAg was chosen to attach the die since it has a low melting temperature of 143 °C. This is contrast to other common die attach solders, that have melting temperatures close to LCP's melting temperature of 315 °C (for example, the melting temperature of gold tin (AuSn) is 280 °C). Since InAg forms a gold-to-gold eutectic bond, a 0.5 μm thin film of gold was evaporated onto the top surface of the copper heat sink. The bottom substrate was attached to the copper heat sink using conductive epoxy, however gold was left exposed in the area of the cavity.

Two Au stud bumps (40 μm tall) were applied to each pad on the Cree die (see Figure 9.3a). This served to both minimize interconnect inductance, as well as to reduce the thermal resistance for heat dissipation. A Finetech Submicron Flip-chip Bonder was used to align the chip to the bottom of S1 and attach it using thermo-compression at 250 °C (Figure 9.3b). Then, S1 was flipped onto S2 while ensuring that the die entered the cavity and attached to the InAg solder. The completed package test structure is shown in Figure



(a) (b) (c)

Figure 9.3. Pictures of the fabricated encapsulated package: (a) stud-bumped GaN die, (a) flip-chip bonded die on the bottom side of the top LCP layer, (c) top-view after encapsulation.

9.3c.

9.1.3 Characterization of the Encapsulated Package

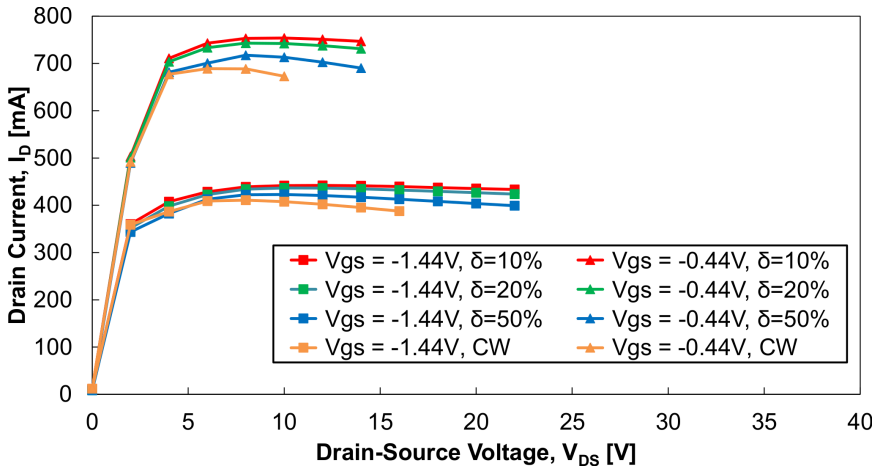
To ensure that the encapsulated package provides enough heat sinking, DC I-V measurements were collected near the maximum current rating for this device (800 mA). These measurements represent a worst case scenario thermally for the die as all of the power is dissipated as heat. Figure 9.4a shows the performance dependence on duty cycle (δ), and it can be seen that the device operates without issue even under continuous bias (CW). To further validate this result, the encapsulated package is compared to a die wire-bonded on AlN at CW in Figure 9.4b. The gate voltages were first tuned at low current levels where self-heating is negligible in order to account for device variability. The results demonstrate that, at high power levels, the encapsulated package performs even better than the wire-bonded sample.

CW S-parameters for the test structure were also measured and compared to simulation at the PA's bias point (Figure 9.5). It is observed that there is very good agreement between the two. In fact, measurements show slightly higher gain at 10 GHz (5.37 dB) than what is predicted in simulation (4.59 dB).

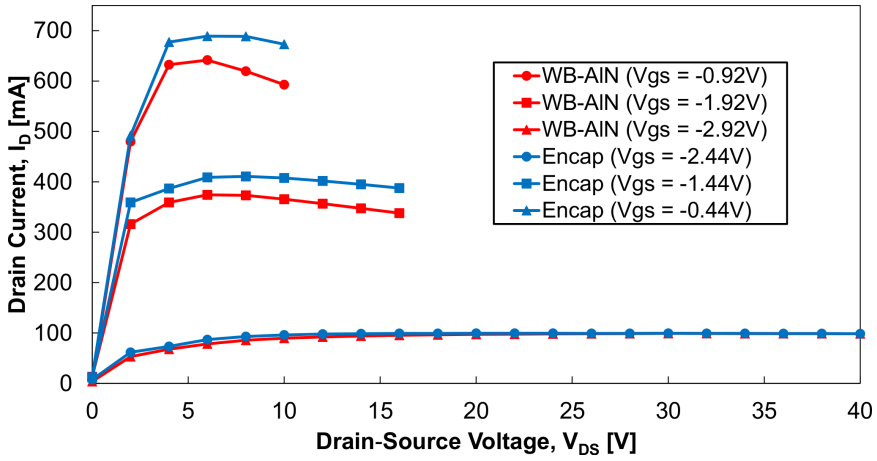
9.1.4 Design of X-Band Encapsulated PA

A center frequency of 10 GHz was chosen for this PA design, as it represents the center of the X-Band. Cree rates the CGHV1J006D HEMT at 6W output power (P_{OUT}) up to 18 GHz. For Class AB configuration, it recommends a drain-source voltage (V_{DS}) bias of 40 V and a drain current (I_D) of 45 mA. This bias point was consequently chosen for this design. Cree also provides a model for this device in Agilent Advanced Design System (ADS), which captures both small-signal and large-signal behavior.

In order to identify the input impedance (Z_{in}) and output impedance (Z_{out}) for optimum P_{OUT} at 10 GHz, source- and load-pull simulations were carried out in ADS for an input power of 27.5 dBm. These were done by importing the simulated small-signal behavior of



(a)



(b)

Figure 9.4. I-V measurements: (a) of the encapsulated package for various duty cycles and at CW, (b) comparing the CW performance of the encapsulated package in LCP versus a device wire-bonded on AlN.

the package transition obtained from HFSS, and treating the package input + die + package output as a single unit. The resulting source- and load-pull curves are provided in Figure 9.6, where, Z_{source} = 3.5 – j33.6 Ω and Z_{load} = 7.6 + j2.2 Ω were found. Under these conditions, the expected performance is G = 9.7 dB, P_{SAT} = 37.2 dBm, PAE = 44%.

Double shunt stub microstrip-based matching networks for the input and output of the PA were designed on the M1 layer. An iterative optimization process involving both ADS and HFSS was used to precisely capture the behavior of the package, the microstrip matching networks and the CPW-to-microstrip transition in between. Figure 9.7a summarizes the stub dimensions and the impedance of the lines. The completed 4.48 mm x 17.15 mm

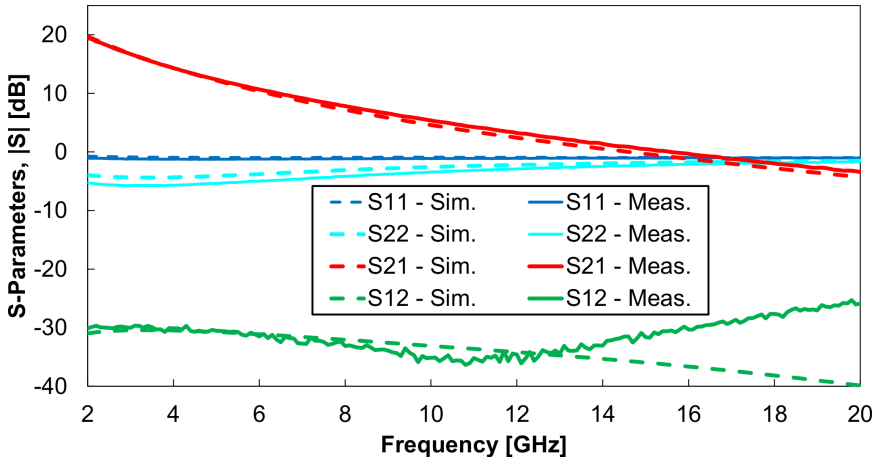


Figure 9.5. Comparison of measured and simulated S-parameters of the test structure at V_{DS} = 40 V and I_D = 45 mA under CW conditions.

encapsulated PA is shown in Figure 9.7b. The aforementioned CPW package structure that forms the core of the PA is also clearly identified.

9.1.5 Characterization of the Encapsulated PA

The small signal frequency response of the power amplifier under continuous (CW) bias is shown in Figure 9.8. Compared to simulation, which showed a peak S_{21} of 15.2 dB at 9.95 GHz, the measured S_{21} experienced a small upward frequency shift, with peak small-signal gain of 14.1 dB now at 10.2 GHz. Similar frequency shifts were also observed for the other S-parameters. This phenomenon is attributed to metal etching tolerances, as well as differences in stud bump height/diameter. This claim is further supported by considering that the abovementioned CW measurement of the stand-alone test structure performed better than simulation. Since both the test structure and the PA were tested under similar thermal conditions (i.e., small-signal CW), it is likely that improved fabrication and adjustments to the package's HFSS model will bring the PA's performance closer to simulation via better impedance matching.

Pulsed S-Parameters under with various duty cycles were also investigated. The difference in $|S_{21,max}|$ from CW to δ = 20% is 0.77 dB, as seen in Figure 9.9a. This is most likely a thermal effect though it is quite minimal. Interestingly, S_{22} at CW showed a slight

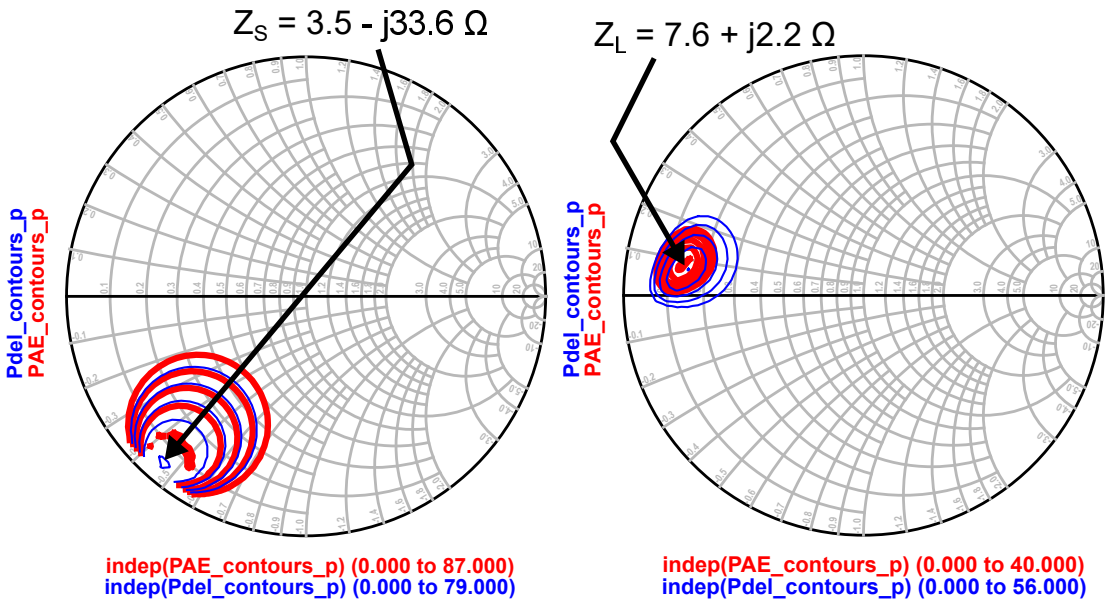
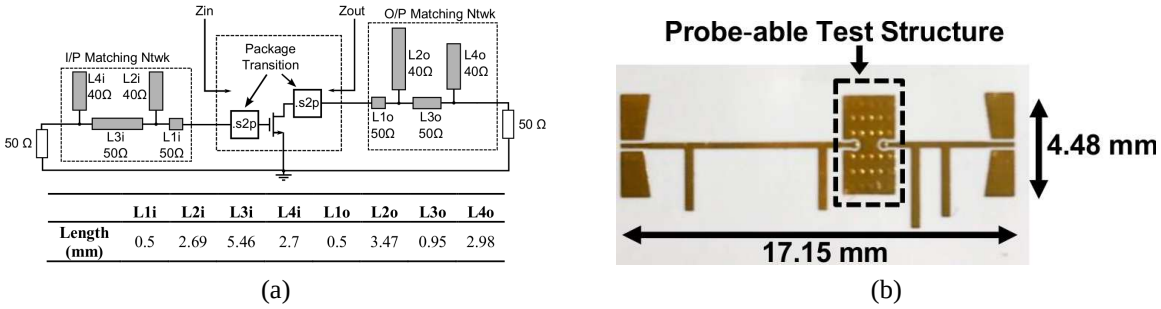


Figure 9.6. Large-signal (a) source-pull and (b) load-pull simulations at 10 GHz used to identify impedance matching conditions for optimum output power.



	L1i	L2i	L3i	L4i	L1o	L2o	L3o	L4o
Length (mm)	0.5	2.69	5.46	2.7	0.5	3.47	0.95	2.98

Figure 9.7. (a) (Top) Schematic of the PA circuit. (Bottom) Table summarizing the lengths of the stubs that make up the input and output matching networks, (b) Top-side image of the fabricated PA.

frequency shift compared to the pulsed S_{22} measurements. This could be related to the device's capacitance and therefore its response to transients experienced under pulsed conditions.

Large signal measurements at CW for the fabricated PA were conducted at 10.2 GHz, since this represented the peak gain frequency. A PAE_{max} of 38% was measured, along with a P_{1dB} of 27 dBm and a P_{SAT} of 37.3 dBm (5.4 W), which indicates that the encapsulated PA approaches the rated 6 W performance specified by Cree. These measurements are shown in Figure 9.10 and compared to large signal simulations at the design frequency

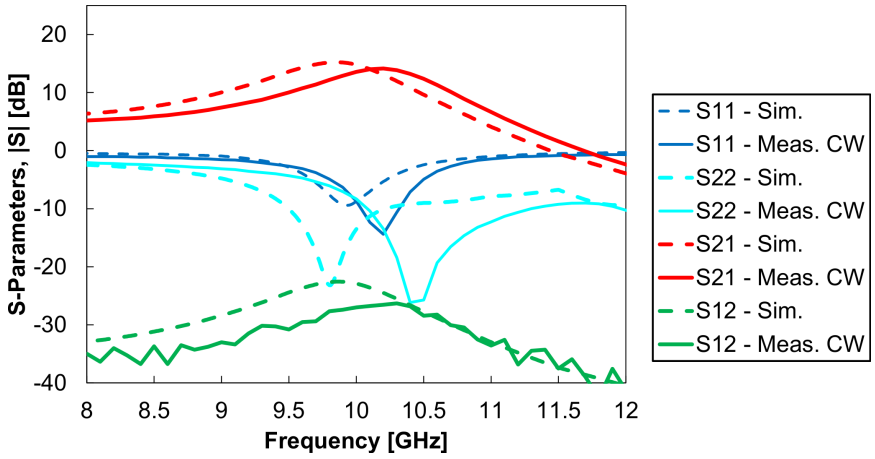


Figure 9.8. Comparison of measured and simulated S-parameters of the encapsulated PA at V_{DS} = 40 V and I_D = 45 mA under CW conditions.

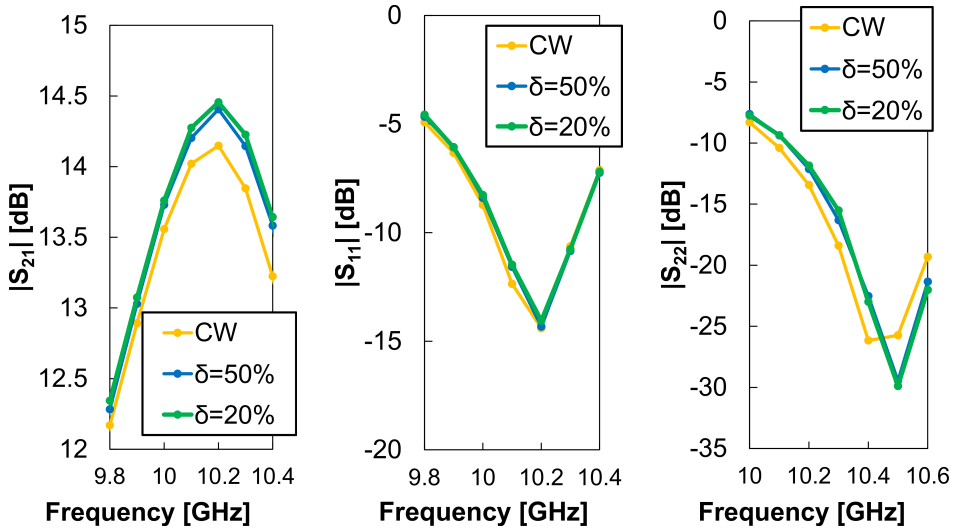


Figure 9.9. Measured dependence of the power amplifier's (a) S_{21}, (b) S_{11} and (c) S_{22} on the duty cycle (δ) (V_{DS} = 40 V and I_D = 45 mA).

of 10 GHz. As explained above, it is believed that the differences between the two can be reduced in the future through tighter process control. Wideband matching can also be implemented in future designs to reduce sensitivity.

Finally, an overview of the PA's large signal performance dependence on pulsed duty cycle is presented in Figure 9.11. As expected, compared to the CW case, pulsed operation increases performance. Operation with δ=50%, for example, yields PAE_{max} = 49%. Though not shown, P_{SAT} at δ = 50% is 38.5 dBm (7 W). Comparison of the measured

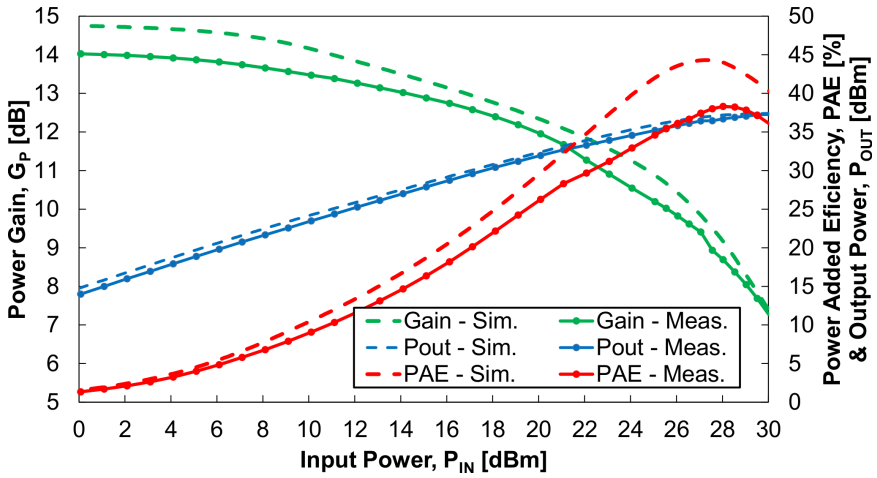


Figure 9.10. Comparison of CW large signal measurements at f = 10.2 GHz and simulated large signal performance at f = 10 GHz.

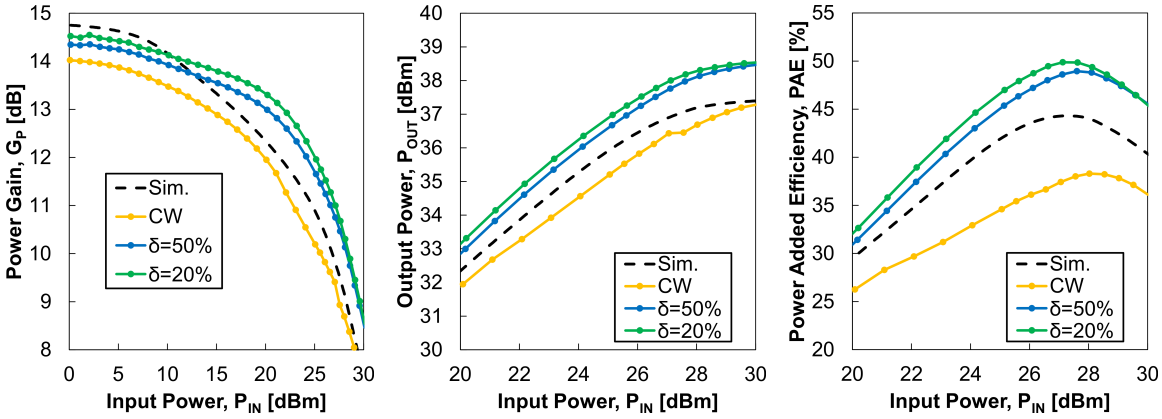


Figure 9.11. Large signal behavior for the encapsulated PA as a function of duty cycle. Results are shown at the peak gain frequencies for simulation and measurement, respectively. (a) Gain, (b) P_{OUT}, (c) P.A.E.

results with the predicted simulated performance indicates that Cree's device model lies in between CW and pulsed performance.

9.2 Conclusion

A fully encapsulated organic package for GaN PAs has been presented. CW operation of the die in this package was demonstrated for the first time, which verified thermal management on par with a traditional AlN substrate. An X-Band PA based on this package was designed, fabricated and measured. At f = 10.2 GHz, it exhibited 38% PAE and P_{SAT} of

5.4 W at CW, or 49% PAE and 7 W P_{SAT} at 50% duty cycle. Now that the thermal and RF performance of this package has been verified, future work will focus on the design of a wideband PA in order to leverage the advantages of the flip-chip interconnect.

CHAPTER 10

ENCAPSULATED ORGANIC PACKAGE TECHNOLOGY FOR WIDEBAND INTEGRATION OF HETEROGENEOUS MMICS

The heterogeneous integration of silicon germanium (SiGe) and gallium arsenide (GaAs) technologies is presented using a novel encapsulated packaging approach with organic laminates. The combination of unique and optimally matched interconnects for each die, and the low-loss nature of the organic substrates, provides wideband performance and system design flexibility. A hybrid receiver front-end is realized on multi-layer Rogers 3003^{TM} to demonstrate this concept, incorporating a flip-chip bonded SiGe low noise amplifier (LNA) and a ribbon-bonded GaAs mixer. The simulated 3-dB bandwidth of the receiver is 4.5-14.5 GHz with a maximum conversion gain of 1.2 dB. Measured results for the packaged module showed a 4-14 GHz 3-dB bandwidth and 0.9 dB maximum conversion gain. These results validate that the package is indeed low-loss and preserves system performance over the entire bandwidth. The receiver also exhibits a DSB NF_{min} of 4 dB and a maximum $P_{1dB,input}$ of -5.5 dBm. This is the first time that heterogeneous semiconductor technologies have been integrated within a multi-layer organic package using different interconnects for each chip to form a receiver. Moreover, the receiver achieves the widest bandwidth among heterogeneous receivers reported to date.

10.1 Introduction

The simultaneous demand for high performance, small form factor, low-weight and low-cost communications systems has driven innovations in both semiconductor and packaging technologies. On the semiconductor front, silicon (Si)-based CMOS offers large scale integration, analog/digital mixed signal capabilities and low cost. Silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) can be directly interfaced with CMOS to create BiCMOS platforms that share the cost and integration benefits of standard CMOS, along

with superior high frequency performance [12,233]. III-V semiconductors, such as gallium arsenide (GaAs) and, more recently, gallium nitride (GaN) offer higher power handling capabilities with the same, if not better, high frequency performance than their Si-based counterparts with the compromise of higher cost and lower levels of integration on chip [88, 234].

As a result, no single technology is currently capable of fulfilling the entire spectrum of application needs, which represents a barrier for the monolithic system-on-chip (SOC) approach. Instead, it is envisioned that next-generation systems will feature heterogeneous integration, whereby different semiconductor technologies are assigned to each functional block depending on their respective strengths (i.e., low-noise performance, mixed-signal integration, high power operation, etc.). DARPA has launched the Diverse Accessible Heterogeneous Integration (DAHI) program to combine III-Vs, MEMS and BiCMOS on a single Si substrate [91, 235, 236]. This approach offers much potential, but at the risk of high implementation cost, and necessitates further technological development. In contrast, the three-dimensional system-on-package (3D SOP) strategy allows for vertical integration of multiple semiconductor active components along with low-loss off-chip passives to achieve both high performance and small form factor [105, 237]. Various packaging material candidates have been investigated, including low temperature co-fired ceramics (LTCC) [106, 107, 238] and organics, such as polyimide, liquid crystal polymer (LCP) and Rogers 3003^{TM}.

Multilayer organic (MLO) packages show much promise due to their low loss [108, 109], low cost, compatibility with large area panel PCB processing and low melting temperature (~300 $^{\circ}C$) compared to LTCC (~850 $^{\circ}C$), which facilitates in-package embedding of active components. Polyimide has been used for chip-scale packages (CSPs), or 3D MMICS, showing high performance and ultra-compact size [239, 240]. In their original form, these packages were constructed directly on top of a single chip or wafer, and therefore could only support one semiconductor technology at a time. Recently, flip-chip based

3D MMICs have also been demonstrated, but have thus far lacked heterogeneous integration of semiconductor technologies [241]. Organic laminates, such as LCP and Rogers 3003^{TM}, have already been demonstrated with CMOS [114], SiGe [115, 116] and GaAs [117] technologies. Due to the thermal management necessary to handle the high-power operation of GaN, organics, which are limited by a low thermal conductivity, were initially overlooked for this technology [242]. Recent work, however, has demonstrated the potential of 3D-SOP techniques with organic laminates for GaN-based applications by incorporating a heat sink into an encapsulated flip-chip package [243]. The performance impacts of reliability concerns, such as fabrication tolerances and laminate alignment errors, have also been studied for multi-layer organic packages [244].

Though previous publications of SOP with organics often mention the potential advantages of heterogeneous integration, their demonstrations have mainly used one or more chips of a single semiconductor technology (e.g., silicon) [245–247]. True heterogeneous integration, consisting of chips of multiple semiconductor technologies embedded in organics, has yet to be implemented in practice to form wideband microwave systems. In response, we present and execute a wideband technique for encapsulating heterogeneous dies within a multi-layer organic package. This approach enables the rapid integration of modules, each relying on different semiconductor chips and/or interconnect methods, to create higher-level functional systems (examples are shown schematically in Figure 10.1). Low-loss and wideband transitions have been realized to preserve chip bandwidth and facilitate module interconnection. The ability to encapsulate the chips increases reliability and adds protection from harsh environments. Chip embedding within organic laminates has been demonstrated in the past, but only with single chips or with narrow bandwidth [114, 116]. To further facilitate the integration of modules, the proposed package is not limited to a single interconnect technology. Moreover, the fabrication can be accomplished with traditional printed circuit board (PCB) manufacturing, and can therefore be scaled to handle large area organic panels to increase throughput.

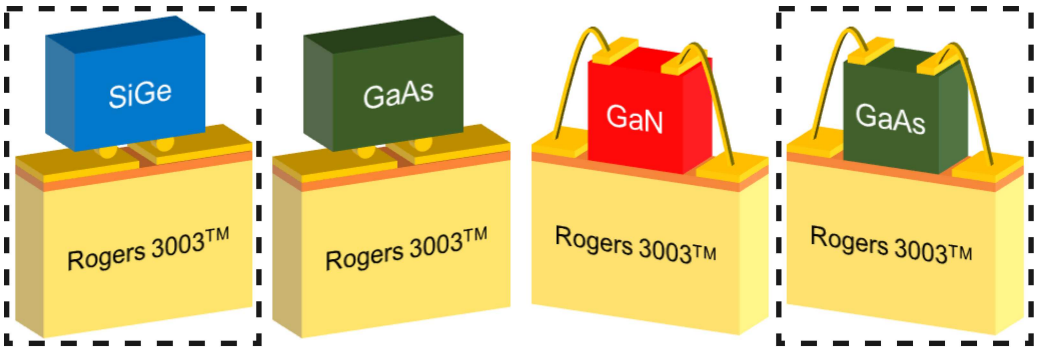


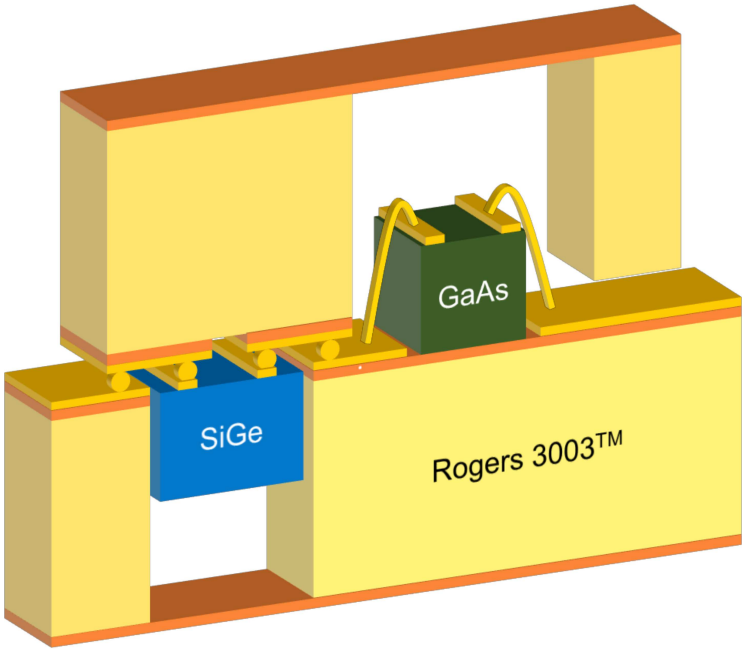
Figure 10.1. Examples of pre-designed modules on organic laminates using chips from various semiconductor technologies and different inter-connect strategies.

As proof of this concept, a hybrid and heterogeneous wideband receiver has been designed, fabricated and thoroughly characterized. It is composed of a flip-chip bonded SiGe BiCMOS low noise amplifier (LNA) and a ribbon-bonded GaAs MESFET double-balanced mixer. Both chips are embedded within an organic packaging laminate (RO3003^{TM}) (see Figure 10.2a). The realized receiver achieves low-loss performance and preserves the bandwidth, covering 4-14 GHz with 0.9 dB maximum conversion gain. This represents the first time that such wideband performance has been achieved in an encapsulated receiver package using more than one semiconductor technology and mixed interconnections.

The paper is organized as follows: Section 10.2 discusses the design of the embedded package. Details are provided about the SiGe LNA and GaAs mixer chips, respectively. Moreover, a comparison between flip-chip bonding and wire-bonding is presented using finite element modeling to understand the impact of interconnect choice on wideband performance. Section 10.3 describes the fabrication of the package, as well as the assembly and die attach processes that were implemented for heterogeneous integration of the SOP receiver. Subsequently, Section 10.4 presents experimental results that were obtained to characterize and therein demonstrate the receiver's wideband performance.

10.2 Encapsulated Package Design

Wideband or multi-band receivers, as shown in Figure 10.2b, can be fully realized using the 3D-SOP approach. This work examines the design of a multilayer organic package



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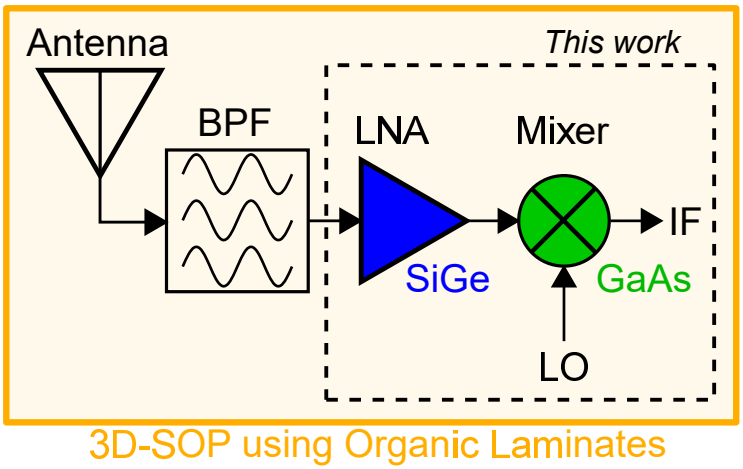


(b)

Figure 10.2. (a) Cross-sectional view of the multilayer receiver package, with embedded flip-chip bonded SiGe LNA and ribbon-bonded GaAs mixer chips (ground lines/bumps are not depicted), (b)Wideband receiver system architecture.

for two heterogeneous LNA and mixer monolithic microwave integrated circuits (MMICs). The characteristics of the SiGe LNA and GaAs mixer are described, along with a design comparison between flip-chip bond and wire-bond interconnect strategies for preservation of the LNA's wideband characteristics. Subsequently, the overall design of the package is discussed. Additional passive components, such as the antenna and band-pass filter, can

be implemented directly on package in the future, where the low loss of the packaging material would allow for higher radiation efficiencies and quality factors, respectively, than on chip [248].

10.2.1 SiGe LNA

The wideband LNA is fabricated using 130 nm SiGe BiCMOS technology with f_T of 200 GHz [249]. Its resistive feedback topology provides a bandwidth of 3-23 GHz, determined by the range of frequencies across which both reflection loss coefficient (S_{11} and S_{22}) remain below -10 dB. Across this band, maximum S_{21} is 9 dB with a gain variation of less than 1 dB. At the lower end of the of the band (i.e., 3-10 GHz), the noise factor (NF) is less than 4.5 dB; across the entire bandwidth NF remains below 6.5dB. The third order intercept point ($IIP3$) is 5.8 dBm, the 1-dB input compression point ($P_{1dB,in}$) is -5.6 dBm. The circuit's power consumption is 33 mW (I_{in} = 10 mA, V_{out} = 3.3 V). The die surface area is 0.48 mm^2, with a thickness of 300 μm.

10.2.2 GaAs Mixer

The passive GaAs double-balanced mixer (Hittite HMC-143), made with a 1 μm GaAs MESFET process, operates from 5 to 20 GHz [250]. The presence of on-chip baluns makes external components and DC bias unnecessary. The IF bandwidth is DC-3 GHz, with a typical conversion loss of 10-12 dB. IF combiners have been used to improve isolation: LO to RF isolation is 26-30 dB and LO to IF isolation is 12-18 dB. IIP3 and IIP2 25 dBm and 50 dBm, respectively, while P_{1dB} = 15 dBm. The single sideband (SSB) NF is 10 dB. The chip's dimensions are 2.1 × 1.45 × 0.1 mm^3. Importantly, Hittite Microwave specifies that the MMIC has been pre-matched on-chip to account for the use of a 3 mil × 0.5 mil gold ribbon bond with a maximum length of 310 μm. Therefore, this type of interconnection should be used for optimal matching and bandwidth.

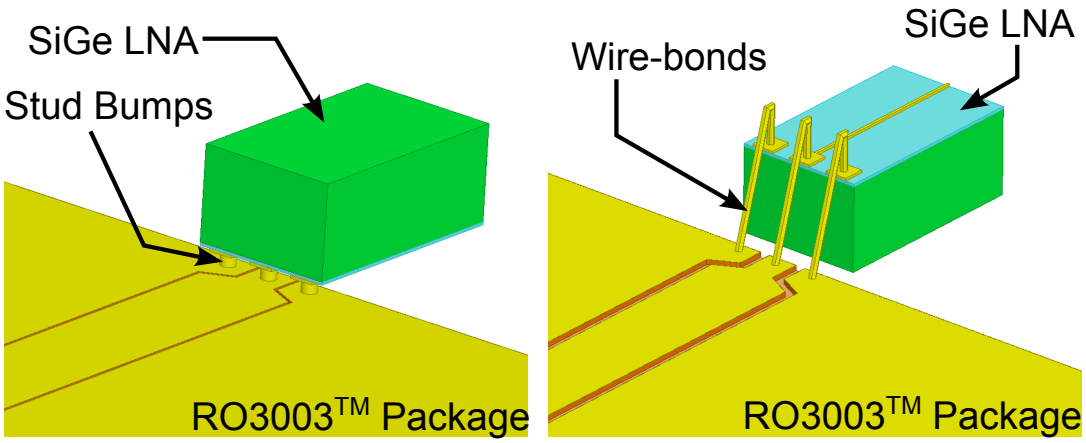
10.2.3 Packaging Laminates: RO3003™

RO3003™, a low-loss ceramic-filled PTFE laminate from Rogers Corporation [251], was chosen as the packaging material for three reasons: 1) low-loss performance with ϵ_r = 3.0 and $\tan\delta$ = 0.001, 2) near-hermetic nature that can preserve embedded dies and 3) availability of suitable thickness. Regarding the latter point, due to the necessity to create cavities to embed the dies, a laminate with a thickness larger than the SiGe LNA's die thickness (300 μm) was required. Liquid crystal polymer (LCP), which has been used extensively in other works, is only available up to 7 mil (175 μm). RO3003™ can be found in thicknesses of 5, 10, 20, 30 and 60 mil. In this work, we use 30 mil (750 μm) to ensure adequate clearance for the dies and increased reliability during the packaging process.

10.2.4 Flip-chip vs. Wire-bond Packaging Effects on wideband LNA performance

Unlike the GaAs chip, whose design includes compensation for the interconnect inductances that are introduced during packaging, the SiGe LNA is only impedance matched on-chip. Therefore, the choice of interconnect type must be carefully considered in order to avoid any deterioration in wideband performance after it has been packaged. Here we consider two interconnection methods – flip-chip bonding and wire-bonding – and simulate these in Ansys HFSS (Figure 10.3).

For the flip-chip method, gold stud bumps with a 50 μm diameter and a 40 μm height were used. The LNA's RF pads are laid out in a ground-signal-ground (GSG) configuration, with a gap of 70 μm and width of 80 μm. In order for the die to be flip-chip bonded, metallic traces that are of the same or similar dimensions are required on package. However, due to the mismatch of ϵ_r and thickness between the 300 μm thick SiGe chip and the 762 μm (30 mil) thick Rogers RO3003™ substrate, it is not possible to design a 50 Ω coplanar wave guide (CPW) on package with the same dimensions as the chip's pads. To minimize the signal trace on package, a gap of 35 μm was used, which is defined by the smallest achievable line-to-line spacing in our fabrication capabilities. This corresponded to a signal width of 302 μm (the presence of an additional RO3003™laminate superstrate was also



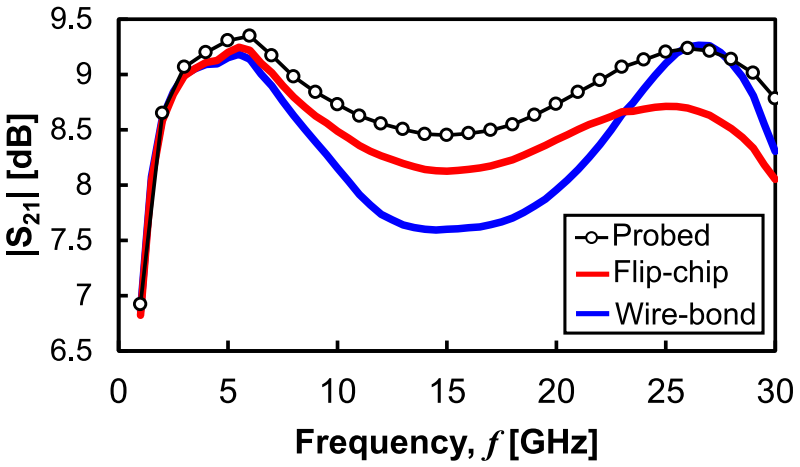
(a) (b)

Figure 10.3. Ansys HFSS Models of Packaged SiGe LNA Chip: (a) Flip-Chip and (b) Wire-Bond Interconnect.

accounted for, but not shown in Figure 10.3). In addition, a transition was designed to further reduce the signal width to 110 μm, enough to allow for proper gold bump placement while keeping the same gap width for fabrication purposes. By minimizing the length of this transition to 170 μm, a near 50 Ω characteristic impedance can be maintained.

For the wire-bond method, the LNA was simulated while sitting on top of the Rogers substrate. Since the LNA does not have a backside ground metal, ground wire-bonds were needed. The wire-bond diameter was 25.4 μm (1 mil) and the distance between neighboring wire-bonds was 150 μm. A loop height of 127 μm was used to minimize the wire-bond length to an estimated 600 μm. This design used the same signal width reduction transition from the flip-chip design to ensure a fair comparison between the two. Though the wire-bonds could have been made longer to avoid this transition, the shorter ground wire-bond length reduces parasitic inductance.

The S-parameter behavior modeled by the HFSS interconnect simulations was transferred to Keysight ADS and used to predict the performance of the packaged LNA. Firstly, it was extracted that the parasitic inductances of the CPW transition plus interconnect are 580 and 300 pH for the wire-bond and flip-chip bond approaches, respectively. This clearly indicates the reduced parasitic inductance introduced by flip-chip bonding. Moreover, from



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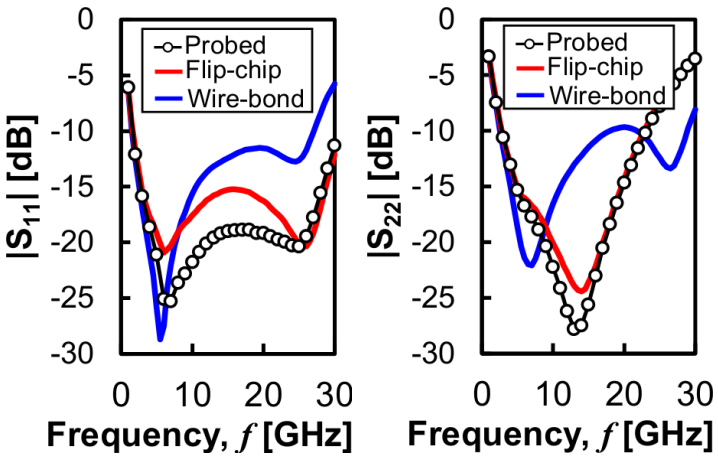

(b) (c)

Figure 10.4. Comparison between on-wafer (meas.), flip-chipped (sim.) and wire-bonded (sim.) small--signal LNA performance: (a) S_{21}, (b) S_{11} and (c) S_{22}.

Figure 10.4, it is observed that the flip-chip bonded LNA has superior performance to the wire-bonded LNA over the wide bandwidth, with better matching and, on average, less gain reduction. The need for extra ground wire-bonds in the wire-bond package presented too large an inductance, resulting in significantly worse matching and gain reduction. Thus, flip-chip bonding was chosen as the preferred packaging method for the SiGe LNA.

10.2.5 Package Design and Layout

Figure 10.2a depicts a cross-sectional overview of the encapsulated receiver package. The received RF signal is fed on the bottom substrate and then passes to the top substrate via

a flip-chip based wideband package-to-package transition. A second package-to-package transition is used to return the amplified RF signal to the bottom substrate, where it is fed to the ribbon-bonded GaAs mixer. The output of the receiver package is the frequency down-converted IF signal. Full embedding of the dies is made possible through the integration of package cavities.

Given the RF properties and thickness of the RO3003^{TM}, 50 Ω CPW lines were designed using Ansys HFSS. As such, the gap (g) and signal line width (w) of the CPW lines on the bottom substrate were 35 μm and 372 μm, respectively. The top substrate's CPW lines were designed with the presence of the bottom substrate as a superstrate taken into account, thus altering the dimensions to g = 35 μm and w = 302 μm.

The package-to-package transition was designed using the same flip-chip method as the package-to-LNA design. Since the difference in signal line width between the top and bottom substrates was only 70 μm in this case, the signal width transition employed in the package-to-LNA transition was not required. Simulation of a back-to-back pair of transitions indicated a total insertion loss lower than 0.097 dB/mm up to 30 GHz. Matching was also good throughout the same bandwidth with S_{11} and S_{22} less than -16 dB.

The layout of the overall receiver board is shown in Figure 10.5. The RF signal input is located at the south side of the board. Next, the signal passes through the SiGe LNA to the subsequent GaAs mixer, where it is mixed with the LO tone fed from the right. The resulting IF signal is measured on the north end of the board. The red traces indicate the M1 metalization layer located on the bottom RO3003^{TM} substrate, whereas the yellow traces show the metal lines on the top substrate (M2). The locations of the RF and DC package-to-package transitions are also indicated. To provide structural support and ensure a good bond between the two laminates, bonding stud bumps were also added outside of the active circuit region. Decoupling capacitors (10 and 100 pF) are connected between the DC bias lines for the SiGe LNA and the neighboring ground plane.

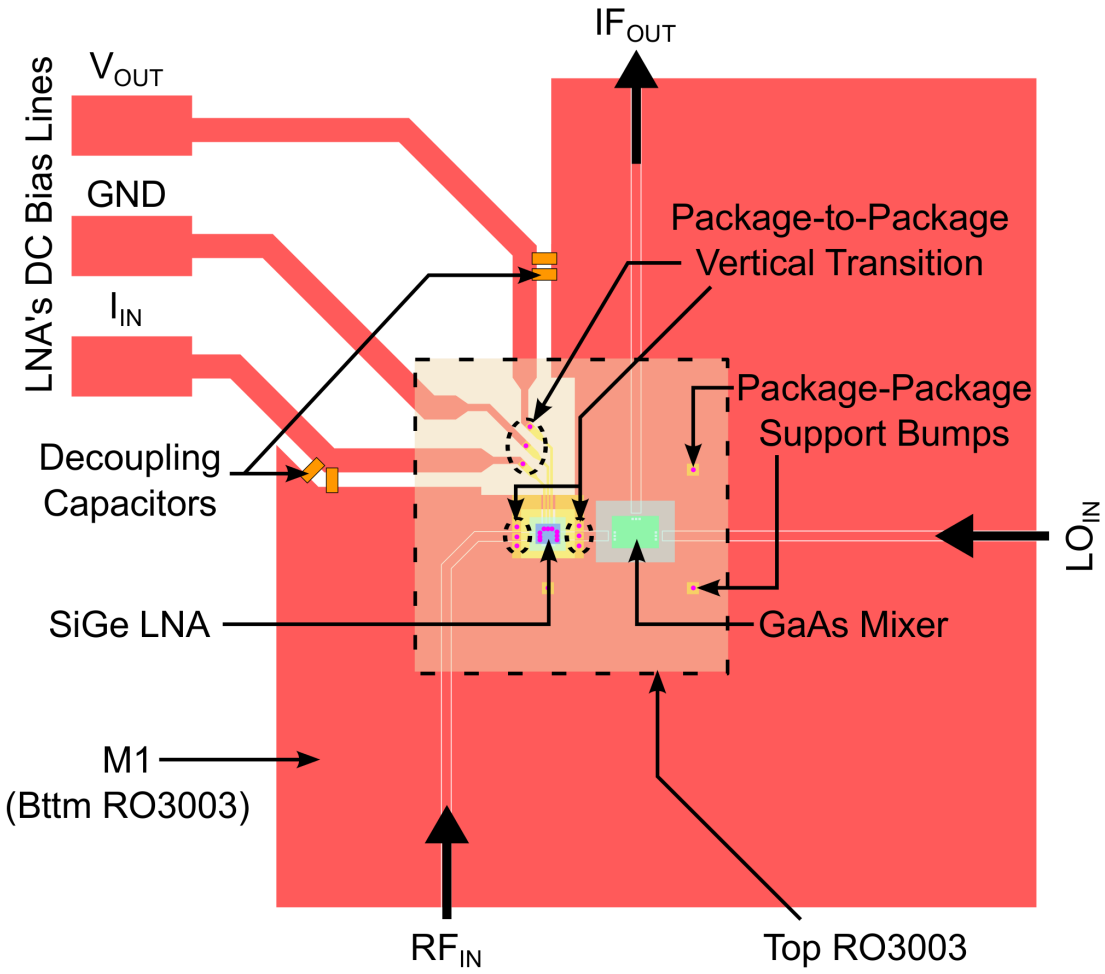

Figure 10.5. Top-view of receiver module layout

10.3 Multilayer Fabrication and Assembly

The receiver was fabricated using 30 mil thick RO3003™, with 18 μm-thick double-clad copper (1/2 Oz.). Figure 10.6 outlines the fabrication and assembly steps that were followed to create the 3D package. Two different types of vias were laser drilled from the bottom of the board: 1) alignment vias that pass through both the RO3003™ as well as the top metal layer, and 2) ground vias that terminate at the top metal layer. The alignment vias were placed only at the outer edge of the substrate to facilitate alignment during the photolithography step. After laser drilling the vias, a thin film of Ti (35 nm)/Au (600 nm) was deposited onto the top surface using electron-beam evaporation. This film is required for adhesion of the gold ribbon bonds and stud bumps, as well as for protection from copper

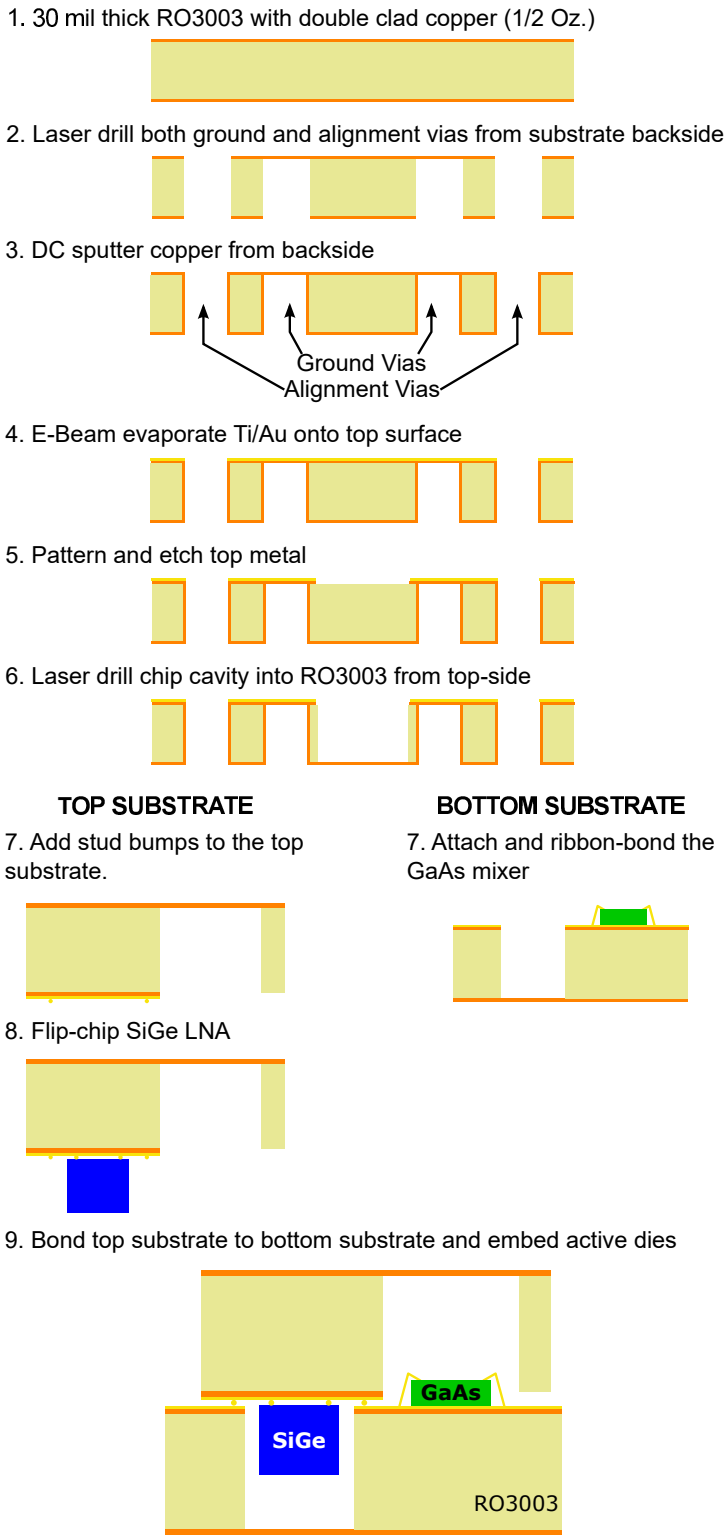

Figure 10.6. Overview of fabrication and assembly process

oxidation. The top Cu/Ti/Au metal stack-up was patterned and etched concurrently using standard photolithography. Rectangular cavities were laser drilled from the top side of the board down to the bottom copper layer.

Gold stud bumps were placed at the ends of the CPW lines on the top substrate using a thermosonic ball bumper. The pads on the SiGe LNA die were also stud bumped using the same approach. Consequently, a Finetech Sub-micron Flip-Chip bonder was used to align and bond the LNA to the top substrate. Silver epoxy was used locally at the pads to promote mechanical adhesion between the board and the die. Meanwhile, 10 pF and 100 pF bypass capacitors were soldered to the bottom board. The GaAs mixer chip was attached to the bottom substrate using silver epoxy. An ultrasonic wedge bonder was used to connect the mixer chip to the board using 3 mil $\times$ 0.5 mil gold ribbons. Finally, the top substrate was flipped and bonded onto the bottom substrate, with both epoxy and the aforementioned bonding bump sites being used to promote the bond strength. Careful alignment was necessary to ensure successful connection of the package-to-package transitions, as well as placement of the dies inside of their respective cavities. Industrially specified front-to-back registration error is 50 μm. Given the width of the signal lines in our designs (300-400 μm), such errors can would still allow the boards to work. Catch pads could also be introduced at the points of transition to improve tolerances in designs where narrower lines are used. Overall, the sequence of fabrication and assembly steps outlined above is scalable and compatible with PCB manufacturing methods.

Figure 10.7 shows a top view of the completed board. Full encapsulation is achieved as the dies are no longer visible, but are instead embedded within the two layer RO3003^{TM} stack up. The dies, packaged using their respective interconnection strategies, can be seen in Figure 10.8, alongside the laser drilled cavities. To conclusively verify the successful integration of the die in the 3D-SOP, an X-ray image was obtained using a Dage XD7600NT X-ray inspection system (see Figure 10.9).

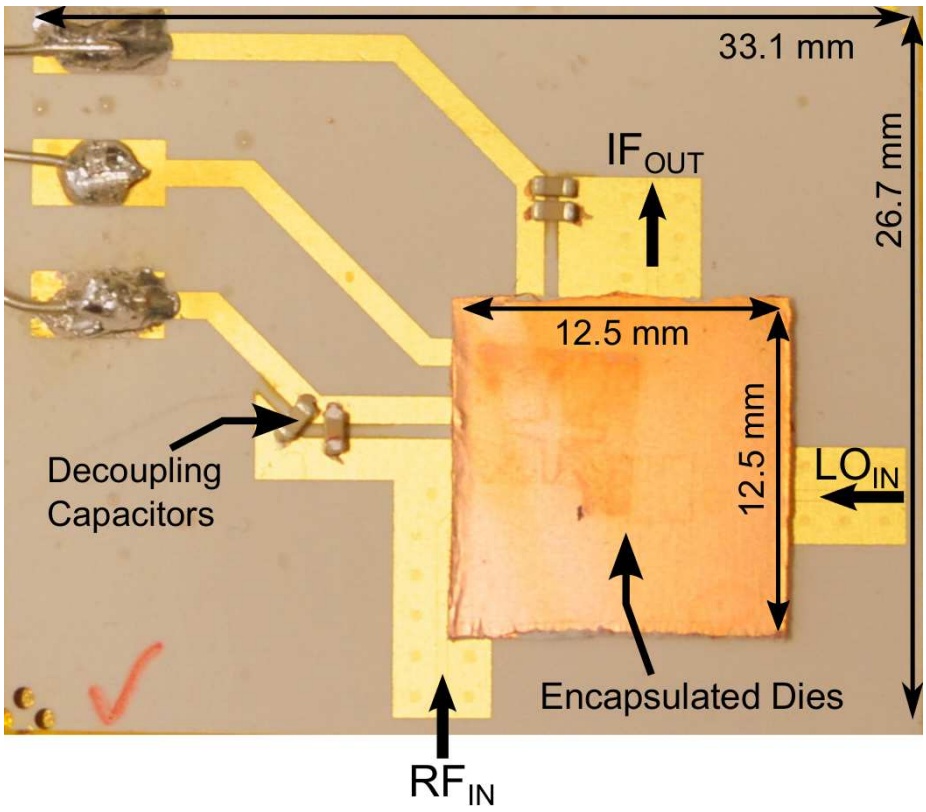

Figure 10.7. Top-View of Completed Board

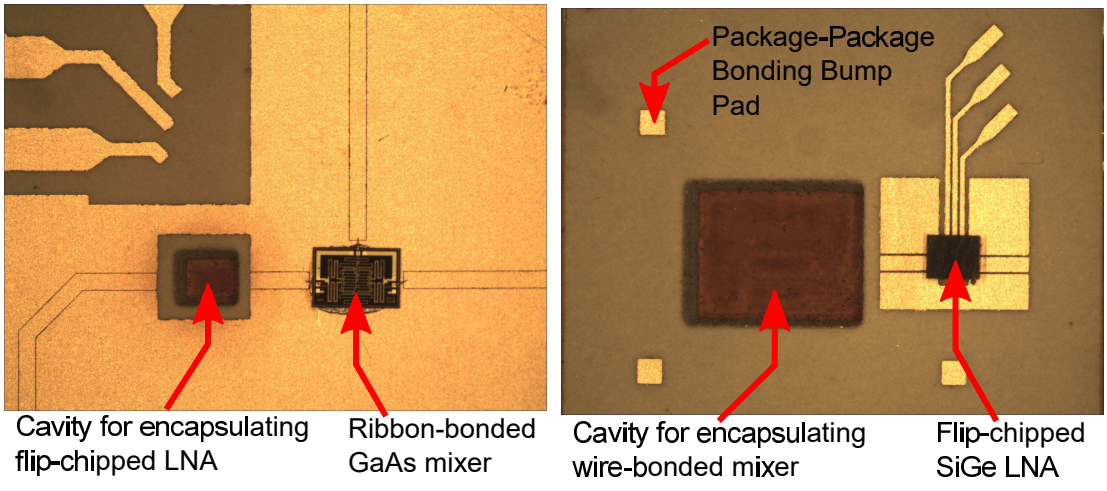

Figure 10.8. Top-view photographs: (a) bottom substrate with ribbon-bonded GaAs mixer and (b) top substrate with flip-chip bonded SiGe LNA.

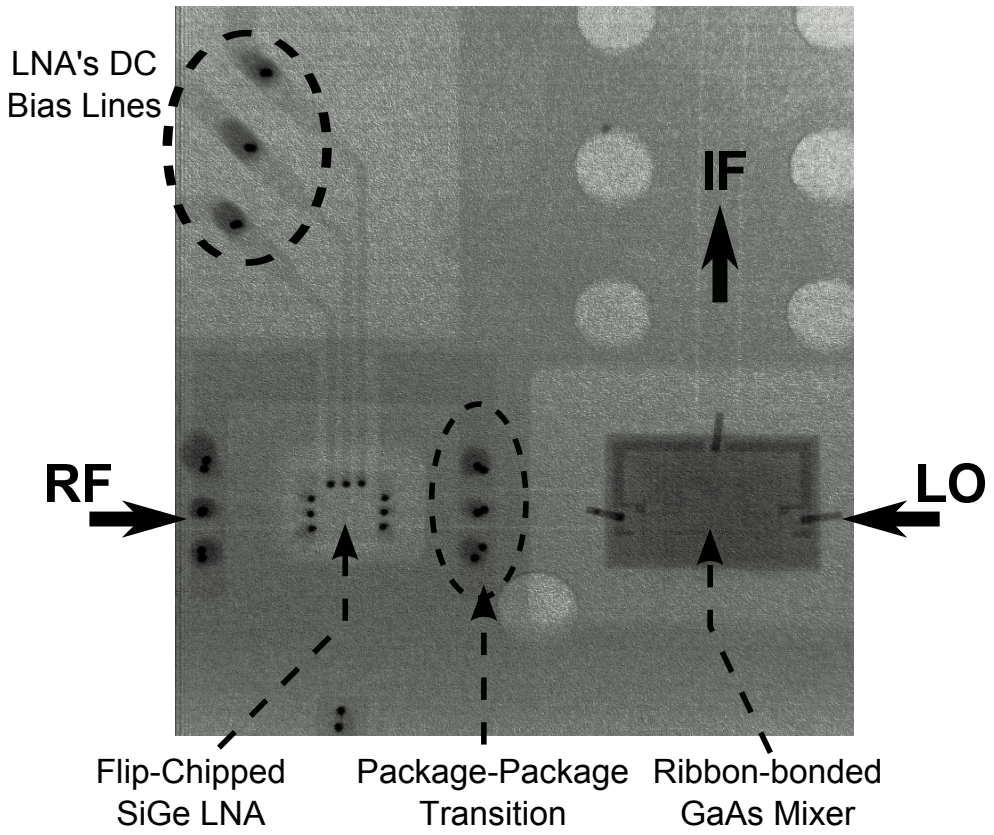

Figure 10.9. X-ray image of the encapsulated package, depicting the heterogeneously interconnected dies.

10.4 Measurements and Results

10.4.1 S-Parameters

The small-signal performance of the package-to-package transition was measured in order to extract the loss per transition. Figure 10.10 shows the response of a back-to-back set of these transitions, consisting of three interconnected CPW sections (i.e., bottom left, top, and bottom right) with a total length of 6.575 mm. Since measurements of the individual CPW lines had been done prior to assembly, it was possible to remove their individual contributions from the total response and consequently estimate the loss per transition as being 0.157 dB at 30 GHz. It can also be seen that the measurements show a shift in resonance compared to the design simulations.

A contact profilometer was used to measure the dimensions of the fabricated lines, and it was found that the gap was smaller than expected: 15-20 μm compared to the design

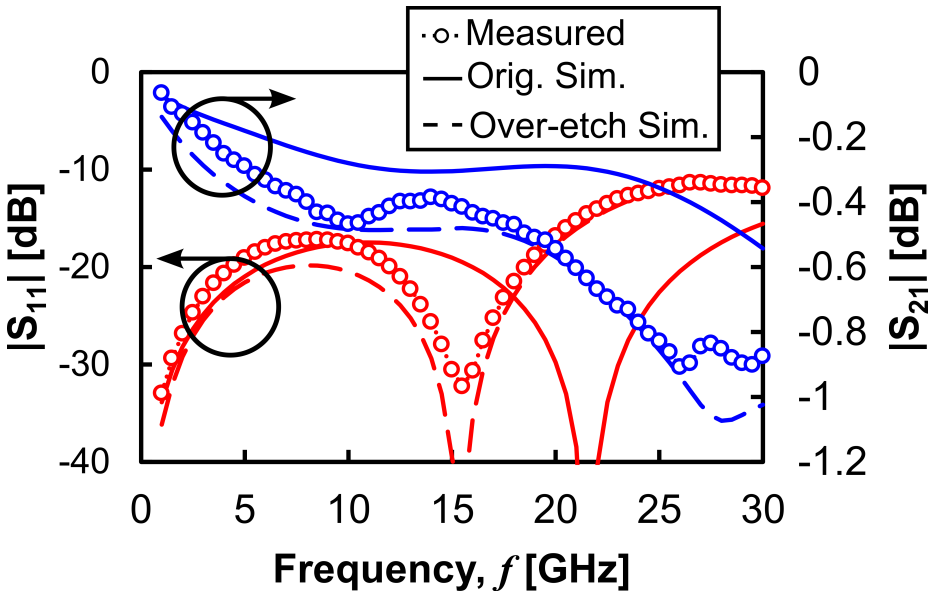

Figure 10.10. S-Parameter response of the package-to-package transition

specification of 35 μm. Simulations with these dimensions were conducted, and agreed with measurement if taking into account different degrees of over- and under-etching of each of the metals (i.e., Cu/Au) in the top metal layer. The difference in thickness between the two metal layers (18 μm vs. 0.6 μm) causes a non-uniform CPW gap in the vertical cross-section.

Figure 10.11 shows the s-parameter response of the flip-chip packaged SiGe LNA. The model for the package die was adjusted to account for over etching, as explained above, and good agreement between measurements and simulation is achieved. The bandwidth of the flip-chip bonded LNA is 3-23 GHz, which is the same as the on-wafer performance. The maximum gain is 8.76 dB, while the gain variation is 0.84 dB. The decrease in gain, particularly at lower frequencies, is explained by the return loss in the package.

10.4.2 Conversion Gain vs. Frequency

An important specification for both mixer and receiver modules is conversion gain (G_C). Figure 10.12 shows measurements obtained for the conversion gain versus RF frequency (f_{IF} = 0.5 GHz). Measurements of the stand-alone mixer reveal that the 3-dB bandwidth of the wire-bonded mixer is 5-15 GHz at P_{LO} = +15 dBm, and 5-20 GHz at P_{LO} = +17 and

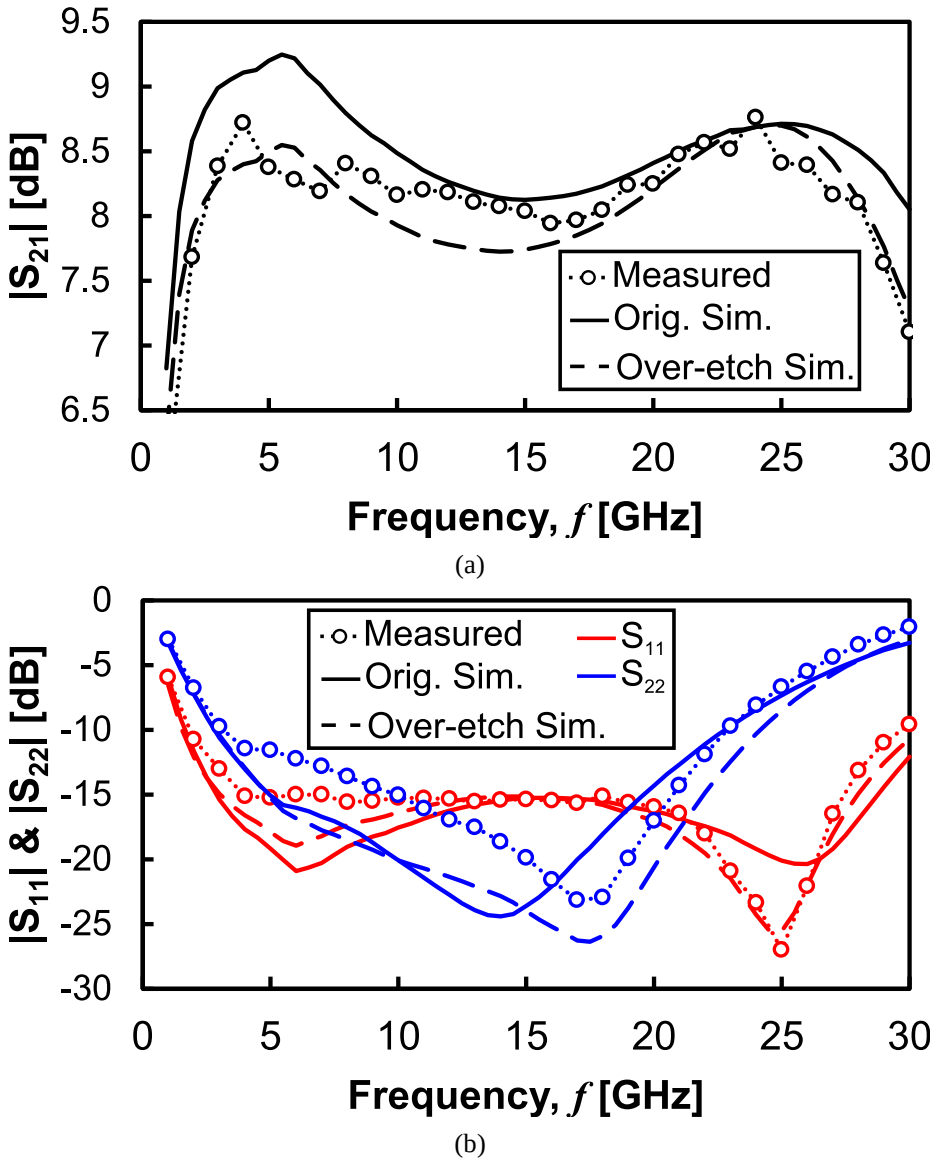

Figure 10.11. Comparison between simulated and measured small-signal performance for the flip-chip bonded LNA: (a) gain and (b) return loss.

+20 dBm. These values are in agreement with Hittite's datasheet [250] and demonstrate that the ribbon bond interconnects do not deteriorate the mixer's gain and bandwidth.

The simulated performance of the full receiver with P_{LO} = +15 dBm shows an approximate 8 dB increase in conversion gain over the stand-alone mixer, which arises from the contribution of the LNA's gain measured above. The predicted bandwidth of the receiver is 4.5-14.5 GHz, with $G_{C,max}$ = 1.2 dB. The reduction in system bandwidth compared to individual chip bandwidth is explained by the LNA's mid-band gain roll-off that out-paces

the mixer's G_C roll-off in the same band. Thus, this effect is not contributed by the package itself and could be improved in the future through the use of an LNA with a different gain profile. Measurements of the full receiver's conversion gain response are in good agreement with simulation. It is found that the measured bandwidth is 4-14 GHz with a $G_{C,max}$ = 0.9 dB. This experimental data shows that the package does indeed preserve the wideband nature of this module, without adding significant losses across the band.

The IF bandwidth of both the receiver and mixer were also investigated by conducting IF frequency sweeps at P_{LO} = +15 dBm for three different RF frequencies (f_{RF} = 5, 8, and 15 GHz). Once again, Figure 10.13 shows the improvement in G_c in the receiver versus the stand-alone mixer. In both cases, the IF bandwidth is 3 GHz, which agrees with Hittite's data sheet-specified performance.

10.4.3 Isolation

Isolation between each of three ports was assessed through measurement (Figure 10.14). For each combination of ports (e.g., RF-to-IF, LO-to-IF, etc.), the power delivered at the output port was measured at the same frequency as the input signal. The RF-to-IF isolation in the mixer alone ranges from 55 dB to 10 dB across the band. After removing the contribution of the LNA's gain, the receiver's minimum RF-IF isolation is only 0.25 dB lower, demonstrating that the package does not have a significant impact. The LO-to-IF isolation, measured using a P_{LO} = +20 dBm, is also largely unchanged for both the mixer and receiver measurements. The maximum isolation is 40.7 dB at 2 GHz, while a minimum of 13.8 dB occurs at 12 GHz. Finally, a P_{LO} = +20 dBm was again used to observe the LO-to-RF isolation behavior. In this case, the LNA's reverse gain (i.e., S_{12}) has been removed and shows excellent isolation.

10.4.4 P_{1dB} Compression vs. RF Frequency

Power sweeps were conducted across the RF bandwidth of the receiver to assess its linearity. In Figure 10.15, the input 1-dB compression point is plotted versus f_{RF} for P_{LO} = +15

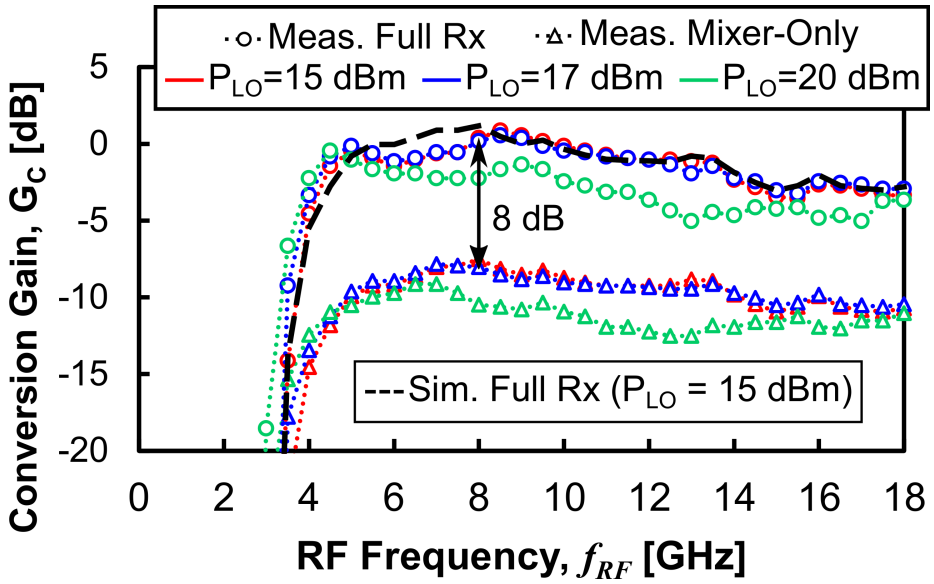

Figure 10.12. Measurement of conversion gain versus RF frequency for various LO power levels, comparing the stand-alone mixer to the fully integrated receiver, and simulation (f_{IF} = 0.5 GHz)

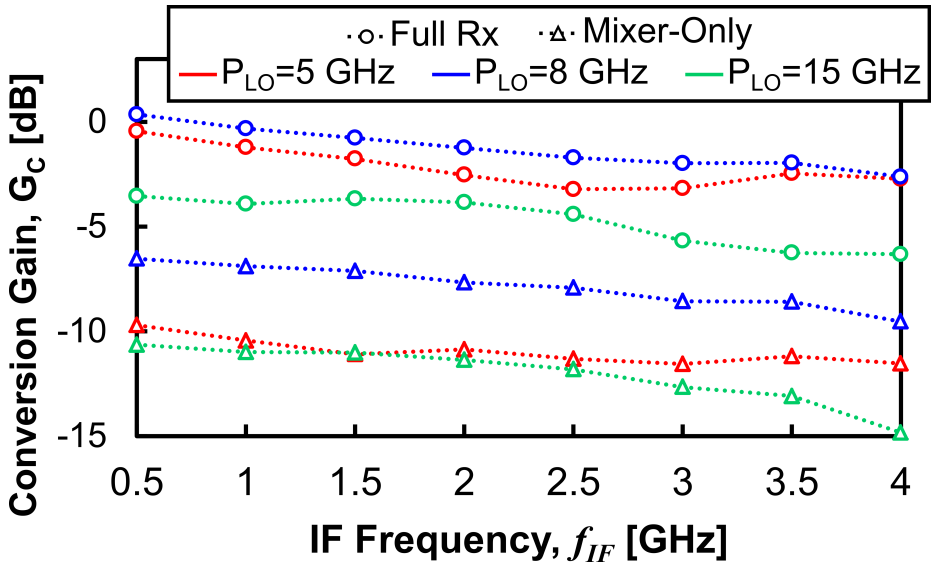

Figure 10.13. Measurement of conversion gain versus IF frequency for various RF frequencies, comparing the stand-alone mixer to the fully integrated receiver (P_{LO} = +15 dBm).

and +20 dBm. Both power levels yield comparable performance. For P_{LO} = +15 dBm, the maximum value of P_{1dB} is -5.5 dBm at 14 GHz. Though not shown here, the GaAs mixer's P_{1dB} is +15 dBm at the same frequency. This change arises from the use of SiGe technology for the LNA. The flexibility provided by the SOP approach makes it possible to interchange technologies in the future in response to each application's specifications.

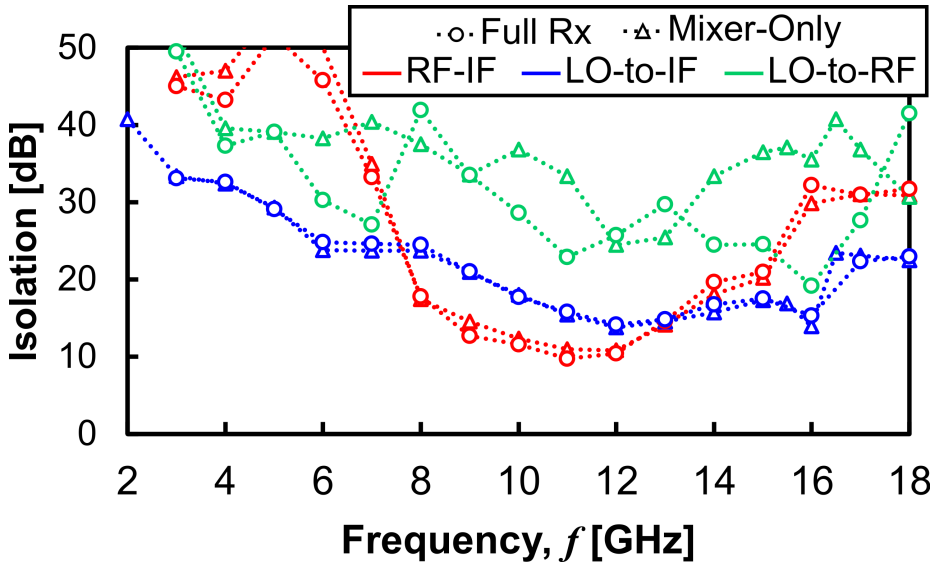

Figure 10.14. Measurement comparison of mixer-only and full-receiver isolation performance. LO–to-IF and LO-to-RF isolation are measured with P_{LO} = +20 dBm**.**

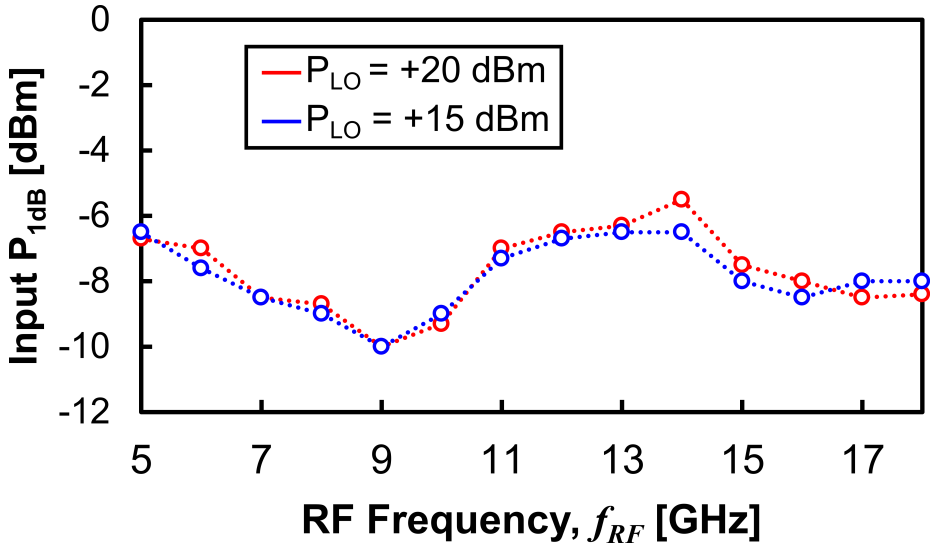

Figure 10.15. Measurement of the input 1-dB **compression point for the packaged receiver module.**

10.4.5 Noise Figure vs. RF Frequency

Figure 10.16 shows the double side band (DSB) noise figure (NF) performance of the receiver. This was measured with an Agilent/Keysight PXA (N9030) using the Y-Factor method under various operating conditions (P_{LO} = +15 and +17 dBm, f_{IF} = 0.5, 1.5 and 3 GHz). As expected, there is an inverse relationship between G_c and NF. That is, as the f_{IF} increases, G_c decreases, which increases NF. Moreover, there is a slight improvement

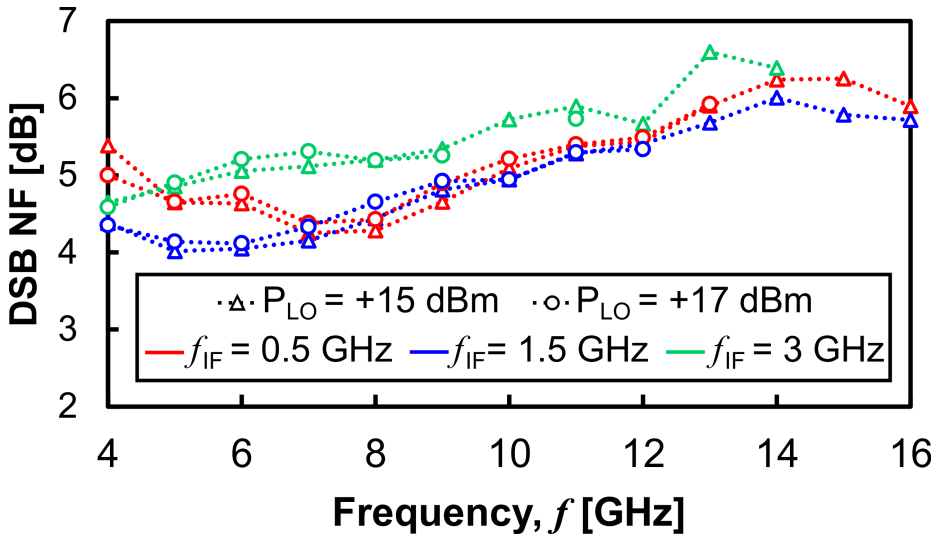

Figure 10.16. Measurement of the receiver's DSB noise figure performance.

in NF when using P_{LO} = +17 dBm compared to +15 dBm. The minimum NF is 4 dB at 5 GHz.

Though often not reported, it is important to consider the uncertainty involved with using the Y-Factor method [252]. By considering the Friis Formula for a two-stage system:

$$F_{TOT} = F_1 + \frac{F_2 - 1}{G_1} \tag{10.1}$$

where F is the Noise Factor and G represents the Gain, it is possible to predict the performance of this receiver. For example, at f = 5 GHz where the minimum NF was measured, F_1 = 2.5, G_1 = 8.4 dB and F_2 = 5. Thus, the estimated receiver's F = 3.1, or NF = 4.91 dB. Keysight offers a method to also calculate the uncertainty of noise measurements based on the characteristics of the device-under-test (DUT) and the equipment used [253]. Hence, at f_{IF} = 5 GHz and f_{IF} = 0.5 GHz, G_C = -0.4 dB, the uncertainty is 1.6 dB. Thus, the measured NF of 4 dB is within the uncertainty range of the predicted performance.

10.4.6 Performance Comparison with Previous Works

A performance summary for the hybrid receiver implemented using our novel packaging approach is presented in Table 10.1 and compared to other SOP receiver examples in the

literature. Our work achieves nearly two octaves of bandwidth (4-14 GHz) and, to the authors' best knowledge, represents the most wideband hybrid and multi-chip receiver. Values for NF_{min} and $P_{1dB,input}$ are also comparable, if not better, than past examples. It should be noted that few papers specify the type of NF that they report (i.e., SSB vs DSB), which makes it difficult to assess performance. Moreover, gain compression ($P_{1dB,input}$) is often overlooked. We observe that only our work and another [254] have successfully encapsulated/embedded chips inside of the package. In both cases, organics were used, which underlines the potential of these materials for 3D-SOP. In contrast to Duo et al.'s approach, our technology relies solely on laminates that are compatible with PCB manufacturing process and therefore does not introduce additional fabrication complexity due to the use of BCB. Moreover, this is the first time that more than one semiconductor technology has been integrated onto a single 3D SOP receiver platform, along with unique interconnect technologies for each MMIC. It should be emphasized that performance improvements to both G_C and NF can be obtained by using an active mixer instead of the passive one used here. Therefore, further work in this area remains promising and open for expansion.

Table 10.1. Comparison of SOP receivers' performance and technology.

Ref.	Frequency [GHz]	Max. Conv. Gain, G_C [dB]	NF_{min} [dB]	$P_{1dB,input}$ [dBm]	Semiconductor Technology	Package Material	Encap? (Y/N)	Interconnect Technology
This Work	4-14	0.9	4*	-5.5	SiGe + GaAs	Organic (RO3003™)	Yes	WB + FC
[240]	9.2-12	25	5**	—	GaAs	Polyimide 3D-MMIC	No	Via Lithography
[255]	1.9	20	3.7**	—	GaAs	Ceramic (Alumina)	No	FC
[256]	24.75-25.25	24.2	4**	—	GaAs	Silicon Wafer + BCB	No	FC
[257]	3-5	18	5.6*	-17.1†	CMOS	PCB (un-specified)	No	WB
[258]	0.3-3	26	3.8**	-18	SiGe	LTCC	No	FC
[254]	5	20	—	—	GaAs	Organic (LCP + BCB)	Yes	Via Lithography
[259]	1-6	25	2.2*	-13.1†	CMOS	Glass + BCB	No	FC

*DSB NF, **Unspecified NF, †Estimated from $P_{1dB,input} \sim P_{IIP3}$ - 9.6 dB [260].

10.5 Conclusion

The successful implementation of an encapsulated packaging method in organics for heterogeneous integration of semiconductor technologies and mixed interconnects has been demonstrated. This packaging approach is low-loss and preserves on-chip wideband performance. The flexibility of interconnect and semiconductor technology choice permit the modular design of systems, each optimized and ready for integration on package. To demonstrate the high performance of this packaging strategy, a wideband receiver has been manufactured. It consists of a flip-chip bonded SiGe LNA and a ribbon-bonded GaAs mixer, encapsulated within low-cost RO3003^{TM} organic laminates. The resulting receiver module exhibited a 4-14 GHz 3-dB RF frequency bandwidth, DC-3 GHz 3-dB IF frequency bandwidth, and a maximum conversion gain of 0.9 dB. To the best of the authors' knowledge, this is the most wideband hybrid receiver to date. The minimum DSB NF is 4 dB, while $P_{1dB,input}$ is -5.5 dBm. This multi-layer SOP demonstration serves as the basis for the development of highly sophisticated and heterogeneous phased array systems, using low-loss organic materials. Future studies will investigate the introduction of high power devices and thermal management techniques, the transition to higher frequency bands that is made possible by the excellent properties of organic laminates and the use of low-inductance flip-chip bonding, in addition to the integration of embedded/low-loss passive components.

CHAPTER 11

CONCLUSIONS AND FUTURE WORK

The objective of this thesis has been to explore the use of wide band gap semiconductors, in particular InGaZnO and GaN, for chemical sensing and wireless electronics. Issues ranging from thin film deposition to device fabrication, from packaging to circuit design and system integration have all been studied. An overview of the fabrication processes used to manufacture the InGaZnO TFT chemical sensors used in this thesis was presented in Chapter 3. This permitted the demonstration of room temperature gas-phase sensing in Chapter 4. Subsequently, two different strategies for liquid phase chemical sensing were investigated. In the first, direct exposure of the InGaZnO TFT to the liquid analyte was explored. This necessitated the passivation of InGaZnO, for which temperature-dependent ALD TiO_x was investigated in Chapter 5. Thus, Chapter 6 demonstrated Super-Nernstian pH sensitivity using low-temperature fabricated InGaZnO double-gated TFTs. In an alternative approach, Chapter 7 leveraged a Zn-ion sensitive and liquid-stable photoluminescent polymer as the chemical sensing layer, and InGaZnO phototransistors were investigated to convert the light into an electrical output. Chapter 8 examined the impact of traditional packaging techniques using an organic LCP laminate on high power GaN transistors. In response to the above discovered performance limitations, a new packaging technique that enabled GaN chip encapsulated within organic laminates was proposed in Chapter 9. This was accompanied by the successful implementation of an encapsulated and flip-chip bonded X-Band GaN/organic PA with multi-watt output power. Lastly, Chapter 10 presented the expansion of the encapsulated organic package concept to realize a wideband receiver using heterogeneous semiconductor chips. What follows in this chapter, is a summary of the major contributions of this thesis, as well as suggestions for future and related research.

11.1 Contributions to InGaZnO TFT-based Bio-Chemical Sensors

InGaZnO thin film transistors (TFTs) have been studied for their use in bio-chemical sensor systems. A low-temperature microfabrication process for these devices was developed using both RF-sputtered and pulse laser deposited (PLD) InGaZnO at room temperature. In order to reduce the voltage of operation, Al_2O_3 deposited using atomic layer deposition (ALD) at 180 °C was chosen as the gate dielectric, which has been shown to combine a high-ϵ_r with low gate leakage current [142]. The first devices made with these materials used an inter-digitated finger layout with large W/L ratios ranging from 106 to 3082. RF-sputtered InGaZnO TFTs with a W/L ratio of 106 exhibited a V_{TH} = 4 V, S = 270 mV/dec, $I_{ON/OFF} \sim 10^{10}$ and $\mu_{FE,SAT}$=5.3 $cm^2\,V^{-1}\,s^{-1}$. By comparison, TFTs with PLD $InGaZnO_{111}$ showed better performance overall: V_{TH} = 1.4 V, S = 230 mV/dec, $I_{ON/OFF} \sim 10^9$ $\mu_{FE,SAT}$ = 6.6 $cm^2\,V^{-1}\,s^{-1}$. Due to the large W/L ratios used by these devices, it was not possible to extract intrinsic performance or study the extent of S/D contact effects.

In response, the device layout was redesigned using a single-channel geometry with a constant channel width of 100 μm and W/L ratios ranging from 1:1 to 50:1. It was found that the W/L ratio significantly affected the mobility of PLD InGaZnO (1:1:5) TFTs, decreasing from >16 $cm^2\,V^{-1}\,s^{-1}$ for L = 100 μm to <4 $cm^2\,V^{-1}\,s^{-1}$ for L = 2 μm. The Transfer Length Method (TLM) was applied to this set of devices to deduce their intrinsic performance, where it was found that the intrinsic mobility is 17.8 $cm^2\,V^{-1}\,s^{-1}$ and the intrinsic V_{TH} is 1.9 V. Importantly, it was also found that R_c (10-100 kΩ) is on the same order of magnitude as R_{ch}. This confirms the significant impact of contact resistance on the extracted extrinsic mobility mentioned above, and leads to the increase of S. To assess process reliability, statistical analysis was conducted on TFTs with a W/L ratio of 10:1 using a common Si p++ gate, a 25 nm Al_2O_3 gate dielectric and two different compositions of PLD InGaZnO (1:1:1 vs. 1:1:5). The InGaZnO (1:1:5) TFTs achieved superior performance (with V_{DS} = 0.1 V), namely V_{TH} = 2.2 ± 0.3 V, $\mu_{FE,LIN}$ = 14.1 ± 1.8 $cm^2\,V^{-1}\,s^{-1}$ and S = 167 ± 42.1 mV/dec, compared to V_{TH} = 2.1 ± 0.3 V, $\mu_{FE,LIN}$ = 3.9 ± 1.1 $cm^2\,V^{-1}\,s^{-1}$

and S = 304 ± 79 mV/dec for the (1:1:1) TFTs.

Overall, the performance and uniformity of the obtained TFTs is sufficient for the chemical sensing applications investigated in this work. The mobility obtained in the PLD InGaZnO (1:1:5) TFTs is higher than that observed in other InGaZnO TFTs fabricated with an ALD Al_2O_3 gate dielectric, where $8 < \mu_{FE} < 10.5$ $cm^2\,V^{-1}\,s^{-1}$ have been reported [142, 261]. However, the values of S and V_{TH} are larger than what has been previously reported: $\sim$ 300 mV/dec vs. 100 mV/dec and $\sim$ 2 V vs. $\sim$ 0.4 V, respectively. This degradation is attributed to the presence of a large R_c, and will be the focus on future work (see below). Nonetheless, these performance traits permit the reliable analysis of chemical sensing.

The stable operation of a sensor is paramount. It is well understood that TFTs, both InGaZnO-based and otherwise [172,174], suffer from positive bias stress-induced threshold voltage shifts. Moreover, it has also been reported that this effect can be mitigated through the use of post-fabrication annealing in an O_2 or wet H_2O atmosphere [162]. In this thesis, annealing and pulsed biasing were applied to gas-phase volatile organic compound (VOC) sensing to improve InGaZnO TFT sensor reliability. It was found that increasing the post-fabrication anneal from 100 °C to 300 °C decreased the change in V_{TH} as a result of 60 min positive bias stress (PBS) from 22% to <5%. Following a 300 °C anneal, the V_{TH} drift was further reduced by decreasing the duty cycle. Specifically, use of a 25% duty cycle reduced the drift to <1.5%; when a duty cycle of 10% was used, the drift came down to <0.5%. When exposed to ethanol vapor to test gas sensing performance, concentrations of 6375 to 25500 ppm induced an average current decrease of 19 pA/ppm. The response was recoverable, which is in contrast to the only other room-temperature InGaZnO TFT gas sensor study [73]. The same study used semi-conducting polymer films to enhance sensitivity, however the conductive nature of the polymers made it unclear whether the current modulation due to gas exposure arose from effects in the InGaZnO, or changes to the polymer itself. In this thesis, an insulating PECH polymer layer was studied instead to

rule out this uncertainty. It was found that it increased sensitivity by 3-4x and inverted the polarity of the response, resulting in a maximum sensitivity of 78 pA/ppm. The decrease in current observed in the exposed bare devices is attributed to oxygen donation from ethanol, which decreases oxygen vacancies and mobility. Similar effects have been reported for TFTs exposed to oxygen vapor [140]. The PECH-coated response, on the other hand, could be due to the accumulation of dipole charge in the PECH that induces an accumulation of carriers in the InGaZnO too. More investigation is required to confirm these hypotheses.

The response to ethanol gas studied above also indicates a second source of instability for InGaZnO TFTs, arising from the interaction at the InGaZnO-air interface. This has successfully been addressed through the addition of passivation films, in particular using organics [84, 185, 186]. The large thickness and low ϵ_r of these films, however, isolates the TFTs to such a degree that they cannot be deployed as chemical sensors. To address this, thin (i.e., nanometer thick) passivation films with high ϵ_r need to be investigated. The studies conducted in this thesis, as well as reports from other groups [85, 194], have shown that the use of PECVD SiO_2/SiN_x and ALD Al_2O_3 passivation can lead to significant negative shifts in V_{TH}. In this thesis, ALD TiO_x passivation was investigated as an alternative material due to its attractive moisture barrier properties and high ϵ_r [188]. It was found that ALD temperature influences post-passivation device performance. Specifically, as the deposition temperature increases, V_{TH} shifts downward and S increases. All of the TiO_x passivated devices were found to have reduced $\mu_{FE,max}$ compared to the bare reference, while higher deposition temperatures offered the highest mobility. Moreover, positive bias stress induced threshold voltage shift was reduced following passivation, indicating that this fabrication step can further add to post-process annealing and pulse mode biasing techniques investigated above to improve bias stress stability. SIMS analysis ruled out the effect of interdiffusion and hydrogen doping as sources of the temperature dependent changes in performance. In stead, it is proposed that temperature-dependent oxygen gettering induces the formation of oxygen vacancies in the InGaZnO film, thus explaining the V_{TH} reduction

post-passivation. To confirm this hypothesis, alternative chemical analysis methods, such as XPS, should be used in the future. Nonetheless, for minimum disturbance to S and V_{TH}, 100 °C TiO_x should be used.

Traditional silicon-based ISFETs have a maximum sensitivity of 59 mV/pH, which is known as the Nernst Limit. Past works have shown that dual-gate TFTs can be used to achieve pH sensitivity beyond the Nernst Limit [79], with sensitivities up to 2 V/pH having been reported [80]. However, these works have all relied on thick, thermally grown SiO_2 in order to minimize the bottom gate capacitance. This high temperature processing step undermines the advantages of using low-temperature semiconductor technologies, such as InGaZnO or organics. In contrast, this thesis has exploited the aforementioned 100 °C ALD TiO_x passivation scheme to achieve a sensitivity of 76 mV/pH. Moreover, it was found that reliable device performance could be maintained over the course of 24 hours within a liquid environment with pH = 5. While these results represent the first demonstration of pH sensitivity beyond the Nernst limit in a device fully fabricated at low temperatures, the measured sensitivity is smaller than what was expected for the used dielectric materials and their thicknesses. Thus, the approaches described in this thesis enable high-sensitivity flexible InGaZnO TFT-based sensors, while calling for future investigation into how the performance can be optimized in the future.

To circumvent the need for passivation, an alternative approach to liquid-phase chemical sensing was also considered. It has been shown that InGaZnO is sensitive to light exposure, and that this response can be amplified through the introduction of p-type polymer films to form phototransistors [43, 221, 222]. In addition, TPN-Cl_2, a photoluminescent polymer, has been shown to be both stable in liquid environments and sensitive to Zn ion concentrations [223]. The two components were combined for the first time to create a 2-stage Zn ion sensing system. The photoresponse of bare InGaZnO TFTs and PQT-12/InGaZnO phototransistors to red light, which is the color of light emitted by the TPN-Cl_2, was investigated, and it was found that the phototransistor showed a 70% higher

sensitivity than the bare TFT. Moreover, when the complete system was assembled, successful detection of 10^{-3} M of Zn ions was recorded.

11.2 Contributions to Hybrid GaN/Organic Microwave Systems

GaN has been leveraged for its high frequency and high power performance that is unmatched by other semiconductor materials. To reduce cost and permit microwave system integration, packaging of GaN devices with organics has been explored, with the following contributions made in this thesis:

Since organics have in large part been overlooked for high power applications, it was necessary to study the thermal and electrical performance of GaN HEMTs packaged in AlN and LCP, with either traditional wire-bonding or flip-chip bonding techniques. The 6 W GaN-on-SiC HEMT die from Cree, CGHV1J006D, was used in these tests. This was executed by employing a combination of IR temperature metrology, as well as examining the effects of self-heating on I-V curves collected via pulsed biasing. It was found that wire-bonded devices on AlN fulfilled their 6 W rating, thus confirming that the high thermal conductivity of this packaging material does not impose thermal restrictions on the device's performance. Devices that were wire-bonded on LCP, however, showed significant degradations in performance, such that 6 W could only be achieved at δ= 10%. Flip-chip bonded devices on AlN showed comparatively favorable performance, with more than 6 W of power capable of being dissipated, even at δ= 50%. Finally, when the die was flip-chip bonded on LCP, severe performance limitations were identified, whereby a maximum average dissipated power of only 0.27 W (with a duty cycle of 10%) could be handled without surpassing the maximum junction temperature of 225 °C specified for the device.

The above quantitatively underlined the difficulty of working with organic laminates when traditional packaging methods are used. In response to this, a novel packaging scheme in organics was proposed that provides adequate thermal management for multi-watt GaN components. This package employs a double flip-chip bonding procedure, whereby

the GaN device is encapsulated within a multi-layer organic stack-up. Finite element modeling was used to minimize package parasitics and facilitate wideband matching network design for hybrid amplifiers. Unlike traditional flip-chip bonding, where the backside of a chip is left unconnected, this package permitted the bonding of the chip's backside to a copper heat sink using low temperature InAg solder. As a result, CW operation of the test die in this package was demonstrated for the first time, which verified thermal management on par with a traditional AlN substrate. An X-Band PA based on this package was designed, fabricated and measured. At 10.2 GHz, it exhibited 38% PAE and P_{SAT} of 5.4 W at CW, or 49% PAE and 7 W P_{SAT} at 50% duty cycle. The output power density of this package is 4.5 W/mm, and is on par or better than competing implementations of hybrid PAs that rely on more expensive substrates, such as AlN, or lossier wire-bonding.

In order to enable the heterogeneous semiconductor technology integration for high performance RF systems, the encapsulated package concept on organics for GaN was extended to SiGe and GaAs chips. The combination of unique and optimally matched interconnects for each die, and the low-loss nature of the organic substrates, provided wideband performance and system design flexibility. A hybrid receiver front-end was realized on multi-layer Rogers 3003^{TM} to demonstrate this concept, incorporating a flip-chip bonded SiGe low noise amplifier (LNA) and a ribbon-bonded GaAs mixer. The simulated 3-dB bandwidth of the receiver is 4.5-14.5 GHz with a maximum conversion gain of 1.2 dB. Measured results for the packaged module showed a 4-14 GHz 3-dB bandwidth and 0.9 dB maximum conversion gain. These results validated that the package scheme was indeed low-loss and preserved system performance over the entire bandwidth. The receiver also exhibits a DSB NF_{min} of 4 dB and a maximum $P_{1dB,input}$ of -5.5 dBm. This is the first time that heterogeneous semiconductor technologies have been integrated within a multi-layer organic package using different interconnects for each chip to form a receiver. Moreover, the receiver achieves the widest bandwidth among heterogeneous receivers reported to date.

11.3 Future Work

This work has investigated a wide range of topics and themes, yielding important results thus far. Nonetheless, a number of interesting opportunities for future research have been identified as a result of the above-described findings:

- **Contact Resistance Reduction**: As unveiled by TLM in Chapter 3, the contact resistance formed between the Cr/Au S/D metalization and the InGaZnO is very large, and leads to a W/L-dependent field-effect mobility. This will need to be reduced in future fabrication iterations to enable high-speed applications. Possible methods of doing this include reducing the Cr thickness from 25 nm to ≤10 nm [165] or using Ti instead of Cr as the adhesive layer [142, 166].

- **InGaZnO TFT fabrication on flexible substrates**: The microfabrication processes developed in this thesis are low temperature and therefore compatible with many flexible and low-cost substrates. Examples of flexible InGaZnO TFTs already exist in the literature, and the field of flexible electronics is rapidly growing. Non-conventional fabrication methods, such as ink-jet printing and soft lithography, should be investigated for InGaZnO. Of particular interest would be to study the compatibility of the materials that are used in these fabrication methods, such as silver nanoparticle-based ink or liquid metal (E-GaIn), with InGaZnO (i.e., contact resistance when forming S/D metalization).

- **New biasing waveforms for stability enhancement:** Duty-cycle controlled unipolar pulse mode biasing has been demonstrated to improve bias stress stability in this thesis. Bipolar pulses should also be investigated to verify whether they can accelerate recovery times. Additional waveforms (e.g., triangular or sinusoidal) may also yield further improvements.

- **Systematic investigation of gas-phase sensing mechanism:** Though VOC sensing has been demonstrated with InGaZnO TFTs, the fundamental mechanism behind

the response requires further analysis. Of major interest is why the polarity of the current response is inverted between the bare TFT and PECH-coated TFT cases. A comparison of different device architectures (i.e., top- vs. bottom-gate) as well as dual-gate devices may shed more light on this, as well as reveal techniques to further improve sensitivity.

- **Improvement in pH sensitivity:** Though pH sensitivity beyond the Nernst Limit has been achieved, further performance improvement can still be sought. The careful selection of the top and bottom-gate dielectrics should be studied to maximize the capacitance ratio, while the pH sensitivity of the top dielectric should also be carefully examined (e.g., use of Al_2O_3 instead of TiO_2).

- **Biofunctionalization of InGaZnO DG-TFTs:** The pH sensors serve as a useful research-level model to understand the performance of DG-TFTs. Going forward, however, true biosamples and biofluids should be investigated. This will involve the use of biofunctionalization protocols to establish selectivity.

- **Implementation of advanced thermal packaging techniques in organics for high power GaN:** Several new thermal dissipation techniques can be investigated to further increase the power handling capability of organic packages for GaN-based RF systems. These include the use microfluidics, or two-phase cooling.

- **Demonstration of wideband GaN PA using encapsulated GaN/organic package:** Though the current work has demonstrated both adequate thermal management, as well as accurate modeling, for the encapsulated package, the use of flip-chip bonding has not been fully exploited yet. A hybrid and wideband PA should be developed with this system to concretely demonstrate the advantages over traditional wire-bonded systems.

- **Heterogeneous T/R Systems in Multi-Layer Organics:** The packaging techniques

developed in this thesis have set the stage for encapsulated, wideband and heterogeneous RF systems in multi-layer organics. They should now be exploited to integrated multiple semiconductor technologies, such as Si CMOS, SiGe, GaAs and GaN, to achieve next generation high-performance microwave and millimeter wave systems.

APPENDIX A

InGaZnO TFT MICROFABRICATION PROCESS

The following is a step-by-step instruction set for fabricating low-temperature InGaZnO thin film transistors (TFTs) in the Georgia Tech Institute for Electronics and Nanotechnology (IEN) cleanroom facilities.

1. **Thermal Oxide Growth**

   - *Tool:* Tystar oxidation furnace (e.g., Mini Tystar 1)
   - *Recipe:* Wet Oxidation (e.g., Wetox.003)
     - Temperature = 1050 °C, Duration: 3 h 30 min
   - Measure Oxide Thickness – Nanospec Refractometer
     - Expected thickness: 10,800 Å or 1.08 μm

2. **Mask 1 - Gate Contact Formation**

   Lift-off is used to pattern the gate metal from Cr/Au, therefore the photoresist must be deposited and patterned prior to deposition. Following deposition of the metal via e-beam evaporation, the photoresist is removed in acetone.

   (a) **Photolithography**

   i. **Spin photoresist**

   - *Tool:* SCS G3P8 Spin Coater
   - *Photoresist:* Futarexx NR9-1500 PY
   - *Recipe:*
     - Step 1: 500 RPM, 5 sec ramp-up (100 RPM/sec), 10 sec hold
     - Step 2: 2000 RPM, 5 sec (300 rpm/sec), 30 sec hold

ii. **Soft bake**

- *Recipe:* 100-110 °C for 3 min on hot plate
- *Expected Thickness:* 1.6 μm

iii. **Exposure**

- *Light Source:* CI-1 (365 nm)
- *Exposure Dose:* 150 mJ cm^{-2}
- *Contact Type:* Hard Contact with 20 μm alignment gap

iv. **Post-Exposure Bake (PEB)**

- *Recipe:* 100-110 °C for 6 min on hot plate

v. **Development**

- *Developer:* RD-6
- *Duration:* 5-7 seconds
- *Clean:* Rinse with DI water for 10 sec and dry with N_2.

vi. **Feature Inspection**

vii. **Descum**

- *Tool:* Plasma-Therm RIE
- *Recipe:* DESC_SPY for 1 minute

(b) **Metal Deposition**

- *Tool:* CHA E-Beam Evaporator or Denton E-Beam Evaporator
- *Recipe:*
  - Pre-Deposition Pressure: $\leq 2 \times 10^{-6}$ Torr
  - Deposit chrome (Cr) at 2 Å/s to achieve thickness of 250 Å.
  - Deposit gold (Au) at 2 Å/s to achieve thickness of 200 nm.

(c) **Lift-off**

- *Preparation:* Glass tub is required. It is preferable that this tub be dedicated for lift-off in order to minimize the risk of contamination. Rinse the tub three times using DI water. Then, rinse it a further three times using acetone. Fill the tub with acetone.
- *Instructions:* Place the wafer inside an acetone bath and let it soak. To avoid acetone evaporation (especially in a fume hood), cover the glass tub using aluminum foil.
- *Duration:* 2-12 hours (the longer, the better)

(d) **Clean Wafer**

i. **AMI Clean:** Using squirt bottles, rinse the wafer using a sequence of acetone, methanol and isopropanol. Thoroughly dry the wafer using an N_2 gun.

ii. **Descum:**

- *Tool:* Plasma-Therm RIE
- *Duration:* DESC_SPY for 4 minutes

(e) **Check Metal Thickness -** Dektak/Tencor Contact Profilometer

3. **Gate Dielectric Deposition**

- **Tool:** Cambridge Nanotech Atomic Layer Deposition (ALD) – Oxide Chamber
- **Material:** Alumina (Al_2O_3)
- **Thickness:** 50 nm
- **Temperature:** 180 °C

4. **InGaZnO Semiconductor Deposition**

- **Tool:** Denton Discovery Sputterer
- **Material:** $InGaZnO_{1114}$

- **Temperature:** Room temperature (no heat applied)
- **Pre-deposition Pressure:** $< 5 \times 10^{-6}$ Torr
- **Sputtering conditions:**
  - *Power:* 150 W
  - *Pressure:* 5 mTorr
  - *Gas:* 100% Ar
  - *Time:* 10 min
  - *Expected thickness:* 50 nm
- **Notes:** Clean deposition chamber prior to each set of deposition runs. This involves removed loose scraps of previously deposited material, in particular copper, and taping the chamber walls with aluminum foil. Pump down will take 12-24 hours to reach required pre-deposition pressure. After this is complete, conduct 2 "seasoning" runs without any samples inside in order to coat the aluminum foil and sample chuck with InGaZnO. These steps will reduce the effects of process cross-contamination. Then, conduct 1-2 test runs in order to confirm deposition rate and uniformity. Thickness measurements can be done using the Woollam Ellipsometer (InGaZnO material recipe is in "Spyros" folder). Be careful to use slow plasma power ramp-up and ramp-down rate (with the shutter closed) in order to reduce risk of damage to the InGaZnO target.

5. **Mask 2 - InGaZnO Mesa Etch**

   (a) **Photolithography**

      i. **Spin photoresist**

         - *Tool:* SCS G3P8 Spin Coater
         - *Photoresist:* Shipley 1813 (SC-1813)

- *Recipe:*
  - Step 1: 1500 RPM, 0.5 sec ramp-up (3000 RPM/sec), 5 sec hold
  - Step 2: 4000 RPM, 1 sec (3500 rpm/sec), 40 sec hold

ii. **Soft bake**

- *Recipe:* 100-110 °C for 100 sec on hot plate
- *Expected Thickness:* 1.6 μm

iii. **Exposure**

- *Light Source:* CI-2 (405 nm)
- *Exposure Dose:* 180 mJ cm^{-2}
- *Contact Type:* Hard Contact with 20 μm alignment gap

iv. **Development**

- *Developer:* MF-319
- *Duration:* 90-120 seconds
- *Clean:* Rinse with DI water for 10 sec and dry with N_2.

v. **Feature Inspection**

(b) **InGaZnO Etch**

- **Etchant:** 300:2 V/V H_2O:Glacial Acetic Acid
- **Temperature:** Room temperature (no heat)
- **Duration:** If using $InGaZnO_{111}$, then 25-35 minutes are required. If using AFRL $InGaZnO_{115}$, then 10-15 minutes are required.

(c) **Clean Wafer**

i. **AMI Clean:** Using squirt bottles, rinse the wafer using a sequence of acetone, methanol and isopropanol. Thoroughly dry the wafer using an N_2 gun.

ii. **Descum:**

- *Tool:* Plasma-Therm RIE
- *Duration:* DESC_SPY for 4 minutes

(d) **Check InGaZnO Thickness** - Dektak/Tencor Contact Profilometer

6. **Mask 3 - Via Opening**

(a) **Photolithography**

i. **Spin photoresist**

- *Tool:* SCS G3P8 Spin Coater
- *Photoresist:* Shipley 1813 (SC-1813)
- *Recipe:*
  - Step 1: 1500 RPM, 0.5 sec ramp-up (3000 RPM/sec), 5 sec hold
  - Step 2: 4000 RPM, 1 sec (3500 rpm/sec), 40 sec hold

ii. **Soft bake**

- *Recipe:* 100-110 °C for 100 sec on hot plate
- *Expected Thickness:* 1.6 μm

iii. **Exposure**

- *Light Source:* CI-2 (405 nm)
- *Exposure Dose:* 180 mJ cm^{-2}
- *Contact Type:* Hard Contact with 20 μm alignment gap

iv. **Development**

- *Developer:* MF-319
- *Duration:* 90-120 seconds
- *Clean:* Rinse with DI water for 10 sec and dry with N_2.

v. **Feature Inspection**

(b) **optional** **Hard Bake:** The Gen 3 mask set contains an annular feature in order to remove photoresist around the outside border of the wafer. This will avoid the Plasma-Therml ICP's clamp from getting stuck on uncured photoresist. If using an older mask set (Gen 1 or 2), then a 30 minute hard bake is required at 100 °C.

(c) **Dielectric Etch**

- *Tool:* Plasma-Therm ICP
- *Recipe:* LAB_C4F8
- *Duration:* 2-2.5 minutes

(d) **Clean Wafer**

i. **AMI Clean:** Using squirt bottles, rinse the wafer using a sequence of acetone, methanol and isopropanol. Thoroughly dry the wafer using an N_2 gun.

ii. **Descum:**

- *Tool:* Plasma-Therm RIE
- *Duration:* DESC_SPY for 4 minutes

(e) **Check Dielectric Thickness** - Dektak/Tencor Contact Profilometer

7. **Mask 4 - Source/Drain Contact Formation**

(a) **Photolithography**

i. **Spin photoresist**

- *Tool:* SCS G3P8 Spin Coater
- *Photoresist:* Futarexx NR9-1500 PY
- *Recipe:*
  - Step 1: 500 RPM, 5 sec ramp-up (100 RPM/sec), 10 sec hold

- Step 2: 2000 RPM, 5 sec (300 rpm/sec), 30 sec hold

ii. **Soft bake**

- *Recipe:* 100-110 °C for 3 min on hot plate
- *Expected Thickness:* 1.6 μm

iii. **Exposure**

- *Light Source:* CI-1 (365 nm)
- *Exposure Dose:* 150 mJ cm^{-2}
- *Contact Type:* Hard Contact with 20 μm alignment gap

iv. **Post-Exposure Bake (PEB)**

- *Recipe:* 100-110 °C for 6 min on hot plate

v. **Development**

- *Developer:* RD-6
- *Duration:* 5-7 seconds
- *Clean:* Rinse with DI water for 10 sec and dry with N_2.

vi. **Feature Inspection**

vii. **Descum**

- *Tool:* Plasma-Therm RIE
- *Recipe:* DESC_SPY for 1 minute

(b) **Metal Deposition**

- *Tool:* CHA E-Beam Evaporator or Denton E-Beam Evaporator
- *Recipe:*
  - Pre-Deposition Pressure: $\leq 2 \times 10^{-6}$ Torr
  - Deposit chrome (Cr) at 2 Å/s to achieve thickness of 250 Å.
  - Deposit gold (Au) at 2 Å/s to achieve thickness of 200 nm.

(c) **Lift-off**

- *Preparation:* Glass tub is required. It is preferable that this tub be dedicated for lift-off in order to minimize the risk of contamination. Rinse the tub three times using DI water. Then, rinse it a further three times using acetone. Fill the tub with acetone.
- *Instructions:* Place the wafer inside an acetone bath and let it soak. To avoid acetone evaporation (especially in a fume hood), cover the glass tub using aluminum foil.
- *Duration:* 2-12 hours (the longer, the better)

(d) **Clean Wafer**

i. **AMI Clean:** Using squirt bottles, rinse the wafer using a sequence of acetone, methanol and isopropanol. Thoroughly dry the wafer using an N_2 gun.

ii. **Descum:**

- *Tool:* Plasma-Therm RIE
- *Duration:* DESC_SPY for 4 minutes

(e) **Check Metal Thickness** - Dektak/Tencor Contact Profilometer

8. **Dicing**

(a) **Spin photoresist**

- *Tool:* SCS G3P8 Spin Coater
- *Photoresist:* SPR-220
- *Recipe:*
  - Step 1: 1500 RPM, 0.5 sec ramp-up, 5 sec hold
  - Step 2: 2500 RPM, 5 sec, 40 sec hold

(b) **Hard bake**

- *Recipe:* 100-110 °C for 20-30 min on hot plate

(c) **Dice** - Dicing Saw with Ni blade

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